Product Specification

(Preliminary)

Part Name: OEL Display Module
Part ID: UG-2833ALBAF01
Doc No.: SAS1-F001-A

Customer:
Approved by

From: Univision Technology Inc.
Approved by

Univision Technology Inc.
8, Kebei RD 2, Science Park, Chu-Nan, Taiwan 350, R.O.C.

Notes:

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2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by Univision Technology Inc. for any intellectual property claims or other problems that may result from application based on the module described herein.

Revised History

Part Number	Revision	Revision Content	Revised on
UG-2833ALBAF01	A	New	September 20, 2005

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Contents

1. Basic Specifications

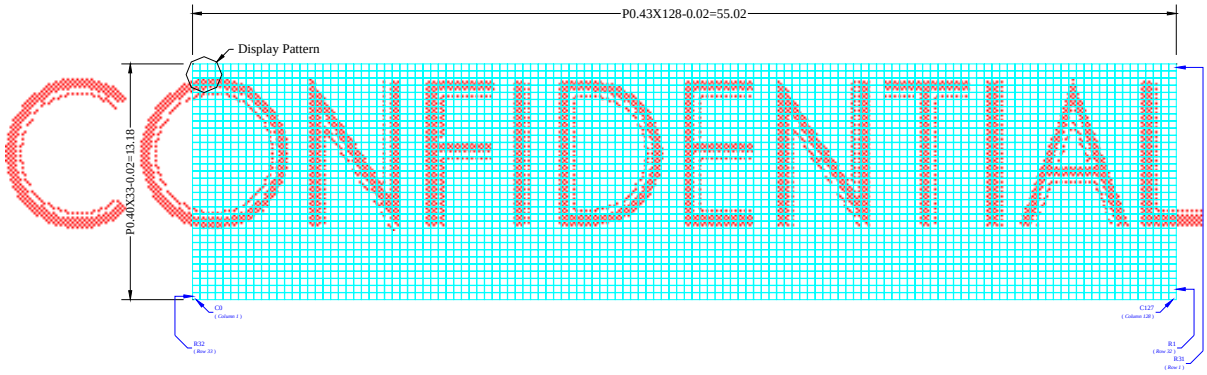
1.1 Display Specifications

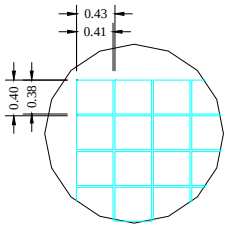
1) Display Mode: Passive Matrix
2) Display Color: Monochrome (Light Blue)
3) Drive Duty: 1/33 Duty

1.2 Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing number
2) Number of Pixels: 128 × 33
3) Panel Size: 62.30 × 22.60 × 2.20 (mm)
4) Active Area: 55.02 × 13.18 (mm)
5) Pixel Pitch: 0.43 × 0.40 (mm)
6) Pixel Size: 0.41 × 0.38 (mm)
7) Weight: 5.7 (g)

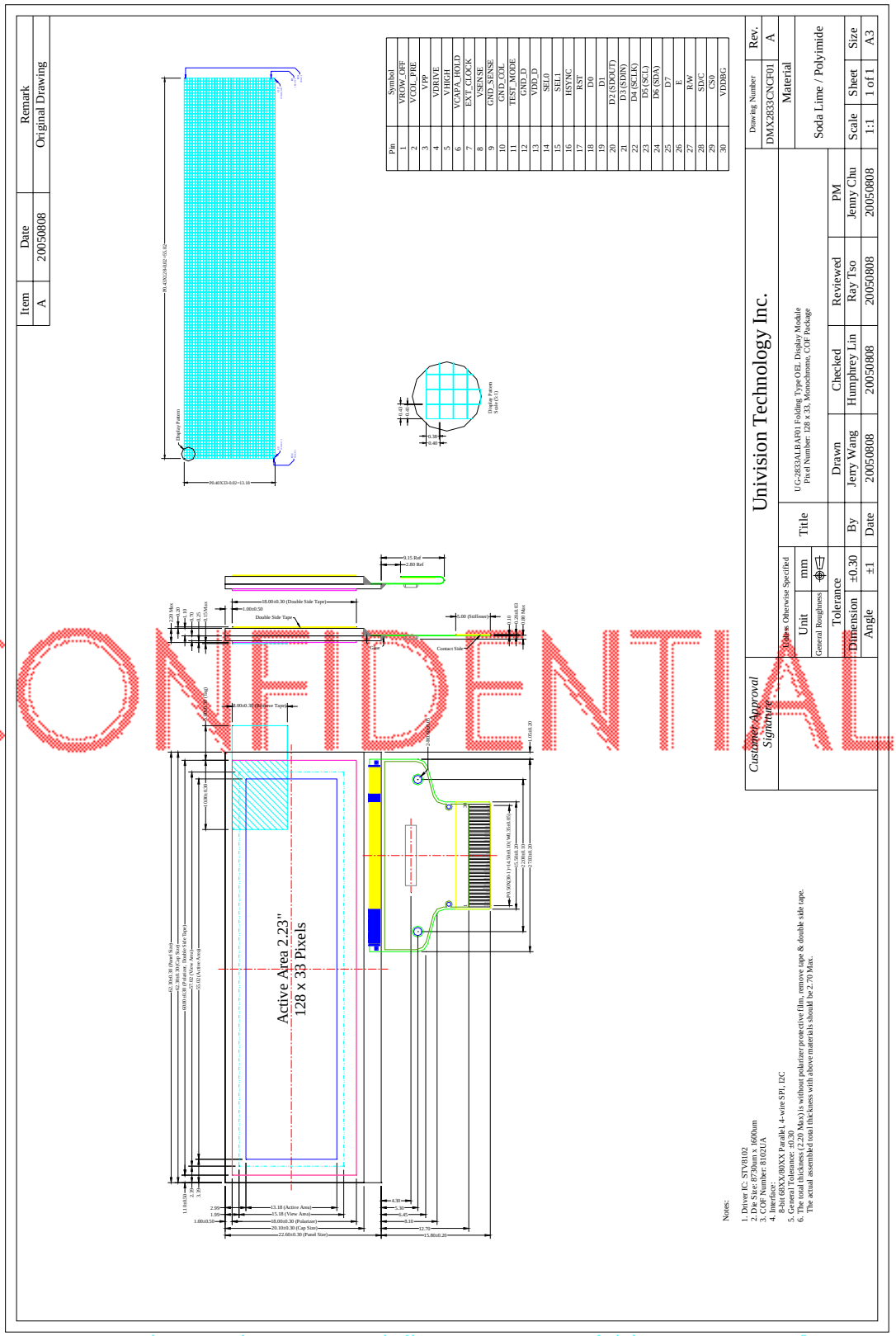
1.3 Active Area & Pixel Construction





Display Pattern
Scale (5:1)

1.4 Mechanical Drawing



1.5 Pin Definition

Pin Number	Symbol	I/O	Function
Power Supply			
13	VDD_D	I	*Power Supply for Logic Circuit* This is the voltage supply pin. It must be connected to external source.
12	GND_D	I	*Ground of Logic Circuit* This is the ground pin. It also acts as the reference for the logic pins. It must be connected to external ground.
3	VPP	I	*Power Supply for OEL Panel* This is the constant current supply pin. It can be supplied externally or generated internally by using internal DC/DC voltage converter.
10	GND_COL	I	*Ground of Column Driver* This is the low level reference voltage for column electrode. It must be connected to external source on ground level or closed to ground.
30	VDDBG	I	*Power Supply for Low Voltage Reference* This is the voltage supply pin. It must be connected to external source.
Driver			
2	VCOL_PRE	I	*Reference Voltage for Column Electrode Pre-Charge Sequence* This is the constant voltage supply pin. It would be supplied externally or be left open while the pre-charge voltage is internally-generated. A tank capacitor should be connected to the VCOL_PRE pin for external setting.
1	VROW_OFF	I	*Reference Voltage for Row Electrode Off-Mode* This is the constant voltage supply pin. It would be supplied externally or be left open while the reference voltage is internally-generated. A tank capacitor should be connected to the VROW_OFF pin for external setting. When display is not active, the row output pins are pulled-up to the off-state voltage.
6	VCAPA_HOLD	I	*Pre-Charge Supply Filtering* This is the voltage supply pin. A capacitor should be connected between this pin and ground.
DC/DC Converter			
4	VDRIVE	O	*Control Signal for Output Voltage Generator* This output pin drives the gate of external power NMOS.
8	VSENSE	I	*Feedback Signal* This pin is the feedback signal for voltage regulation loop. It is used to adjust the booster output voltage level (VPP). In case of VSENSE feedback disconnection the Driver is switched off.
5	VHIGH	I	*High Voltage Step-up Circuit* This pin is the feedback signal for voltage regulation loop. It is used to adjust the booster output voltage level (VPP). An internal NMOS transistor connected between pins VHIGH and VDRIVE allows VPP to raise until the voltage on pin VDRIVE (stemming from VPP) is high enough to switch the external NMOS transistor.

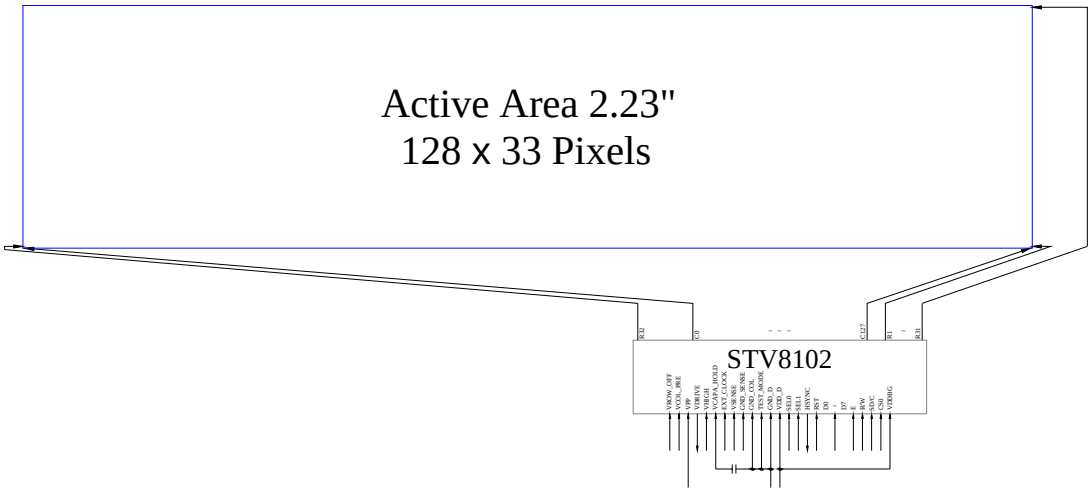
1.5 Pin Definition (Continued)

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4">DC/DC Converter (Continued)</td></tr>
<tr><td>9</td><td>GND_SENSE</td><td>I</td><td>Ground of Current Detection
This pin is the feedback signal for current sense. It is used for current detection for step-up circuitry.</td></tr>
<tr><td colspan="4">Clock</td></tr>
<tr><td>7</td><td>EXT_CLOCK</td><td>I</td><td>External System Clock Source
This pin is the system clock input. When internal clock is enabled, this pin should be left open. Nothing should be connected to this pin. When internal clock is disabled, this pin receives display clock signal from external clock source.</td></tr>
<tr><td colspan="4">Testing Pads</td></tr>
<tr><td>11</td><td>TEST_MODE</td><td>I</td><td>Test Mode Select
This is reserved pins for IC testing. It must be connected to ground for normal status.</td></tr>
<tr><td>16</td><td>HSYNC</td><td>O</td><td>Horizontal Synchronization Triggering Signal
This pin will send out a signal that could be used to identify the driver status. It should be left open individually.</td></tr>
<tr><td colspan="4">Interface</td></tr>
<tr><td>14
15</td><td>SEL0
SEL1</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>68XX-parallel</th><th>80XX-parallel</th><th>Serial</th><th>I2C</th></tr>
<tr><td>SEL0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>SEL1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>17</td><td>RST</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>29</td><td>CS0</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS0 is pulled low.</td></tr>
<tr><td>26</td><td>E</td><td>I</td><td>Read/Write Enable or Read
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS0 is pulled low.
When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS0 is pulled low.</td></tr>
<tr><td>27</td><td>R/W</td><td>I</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W) selection input. Read mode will be carried out when this pin is pulled high and write mode when low.
When 80XX interface mode is selected, this pin will be the Write (WR) input. Data write operation is initiated when this pin is pulled low and the chip is selected.</td></tr>
</table>

1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
Interface (Continued)			
28	SD/C	I	*Data/Command Control* This pin is Data/Command control pin. When the pin is pulled high, the data at D7~D0 is treated as display data. When the pin is pulled low, the data at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
18~25	D0~D7	I/O	*Host Data Input/Output Bus* These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D3/D2 will be the serial data input/output (SDIN/SDOUT) and D4 will be the serial clock input (SCLK). When I2C mode is selected, D5 will be the clock signal (SCL) and D6 will be the I2C data input (SDA). Refer to the configuration of I2C interface.

1.6 Block Diagram



MCU Interface Selection: SEL0 and SEL1
Pins connected to MCU interface:
RST, D0~D7, SD/C, WR, and CS0

2. Absolute Maximum Ratings

2.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage	V_{DD_D}	-0.3	4.6	V	1, 2
Driver Supply Voltage	V_{PP}	-0.3	22	V	1, 2
Operating Temperature	T_{OP}	-20	70	°C	-
Storage Temperature	T_{STG}	-30	80	°C	-

Note 1: All the above voltages are on the basis of "GND = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

2.2 Regarding the Gradation

Although this module possesses the gradation function, respective gradation levels will vary depending on the production conditions etc. Also, the temperature range where the gradation function can be guaranteed will be -10°C~60°C.

3. Electrical Characteristics

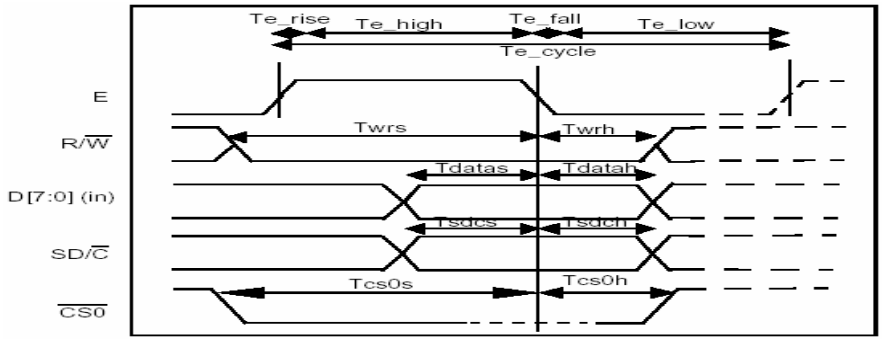
3.1 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD_D}		1.8	3.3	3.6	V
Driver Supply Voltage	V_{PP}		-	12	-	V
High Level Input	V_{IH}		$0.7 \times V_{DD\_D}$	-	V_{DD_D}	V
Low Level Input	V_{IL}		GND	-	$0.3 \times V_{DD\_D}$	V
Column Low-Voltage Reference	V_{COL_GND}	V_{DD_A} = 3.3V V_{DD_A} = 1.8V	0 0	-	1.5 0.4	V

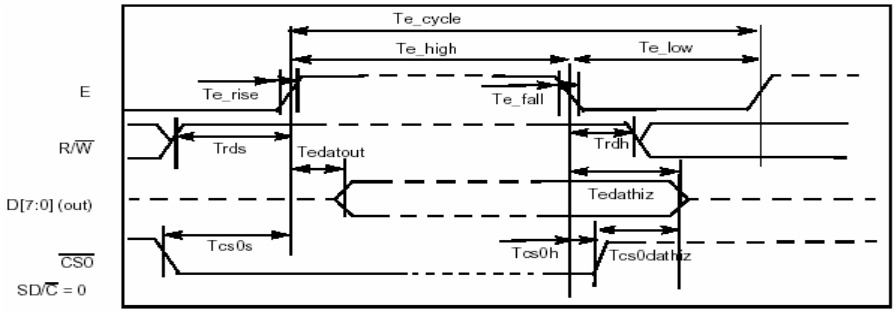
3.2 AC Characteristics

3.2.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Typ	Max	Unit
T_{e_cycle}	System Cycle Time	300	-	-	ns
T_{e_low}	Write Low Pulse Width Read Low Pulse Width	60 120	-	-	ns
T_{e_high}	Select High Pulse Width	60	-	-	ns
T_{e_rise} T_{e_fall}	Rise Time Fall Time	-	-	15 15	ns
T_{wrs} T_{wrh}	Write Data Setup Time Write Data Hold Time	TBD	50 50	-	ns
T_{rds} T_{rdh}	Read Setup to E Rising Edge Read Hold from E Falling Edge * CL = 100pF	TBD	50 50	-	ns
T_{datas} T_{datah}	Data Address Setup Time Data Address Hold Time	25 25	-	-	ns
$T_{edatout}$	Data Output from E Rising Edge	-	20	TBD	ns
$T_{edathiz}$	Data Hiz from E Falling Edge	-	-	TBD	ns
$T_{cs0dathiz}$	Data Hiz from CS0 Rising Edge	-	-	TBD	ns
T_{sdcs} T_{sdch}	SD/C Setup Time SD/C Hold Time	TBD	60 60	-	ns
T_{cs0s} T_{cs0h}	Chip Select Setup Time (Write) Chip Select Hold Time	TBD	120 60	-	ns
T_{cs0s} T_{cs0h}	Chip Select Setup Time (Read) Chip Select Hold Time	120 60	-	-	ns



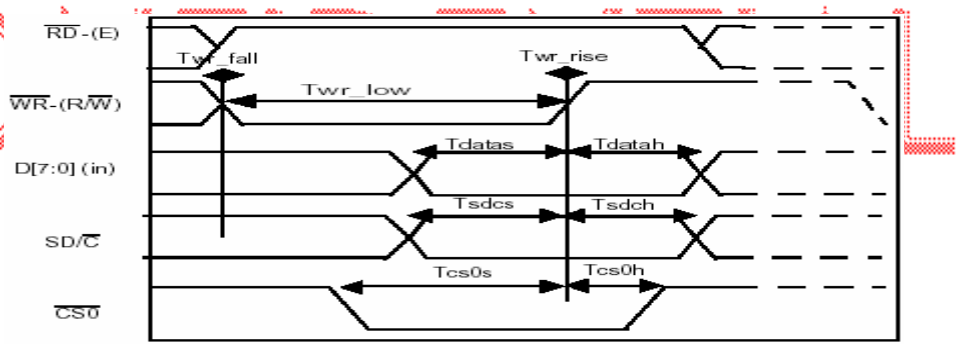
Timing Diagram for Write Mode



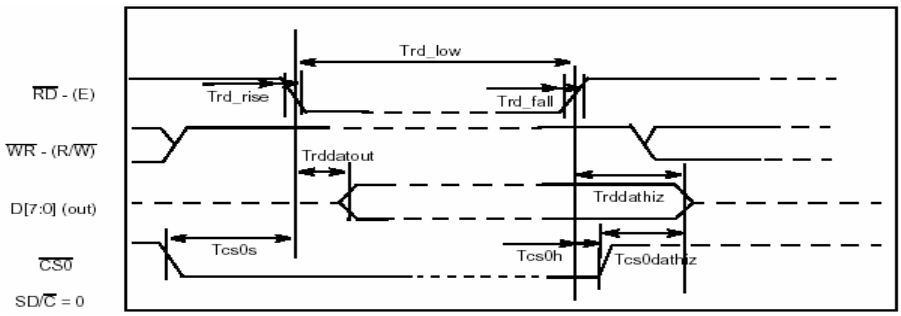
Timing Diagram for Read Mode (Register Only)

3.2.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Typ	Max	Unit
T_{wr_low} T_{rd_low}	Write Low Pulse Width Read Low Pulse Width	60 120	-	-	ns
T_{wr_rise} T_{rd_rise}	Rise Time	-	-	15	
T_{wr_fall} T_{rd_fall}	Fall Time	-	-	15	ns
T_{datas} T_{datah}	Data Address Setup Time Data Address Hold Time	25 25	-	-	ns
$T_{rddatout}$	Data Output from RD Falling Edge * CL = 100pF	-	20	TBD	ns
$T_{rddathiz}$	Data Hiz from RD Rising Edge * CL = 100pF	-	-	TBD	ns
$T_{cs0dathiz}$	Data Hiz from CS0 Rising Edge	-	-	TBD	ns
T_{sdcs} T_{sdch}	SD/C Setup Time SD/C Hold Time	TBD	60 60	-	ns
T_{cs0s} T_{cs0h}	Chip Select Setup Time (Write) Chip Select Hold Time	TBD	120 60	-	ns
T_{cs0s} T_{cs0h}	Chip Select Setup Time (Read) Chip Select Hold Time	120 60	-	-	ns



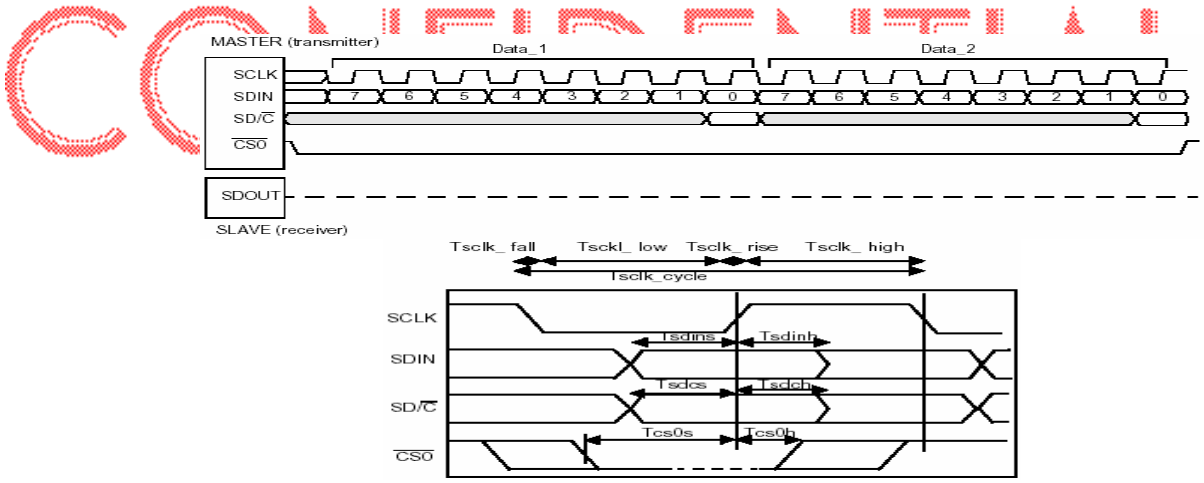
Timing Diagram for Write Mode



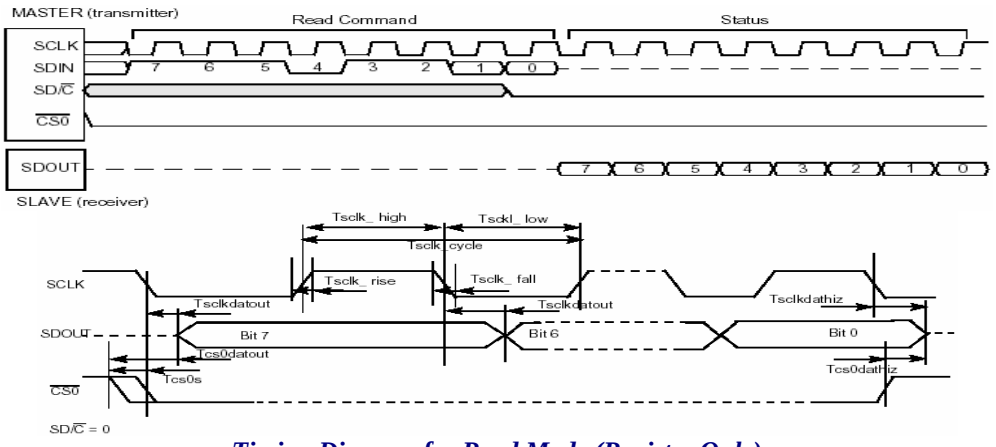
Timing Diagram for Read Mode

3.2.3 Serial Interface Timing Characteristics:

Symbol	Description	Min	Typ	Max	Unit
T_{sclk_cycle}	Serial Clock Cycle Time	250	-	-	ns
T_{sclk_low}	Write/Read Low Pulse Width	100	-	-	ns
T_{sclk_high}	Select High Pulse Width	100	-	-	ns
T_{sclk_rise} T_{sclk_fall}	Rise Time Fall Time	-	-	15 15	ns
$T_{sclkdatout}$	Data Output Time after SCLK Falling Edge	TBD	50	-	ns
$T_{sclkdathiz}$	Data Output Hiz State Time after SCLK Falling Edge	TBD	50	-	ns
$T_{cs0datout}$	Data Output Time after CS0 Falling Edge	TBD	50	-	ns
$T_{cs0dathiz}$	Data Output Hiz State Time after CS0 Rising Edge	TBD	50	-	ns
T_{sdins} T_{sdinh}	SDIN Setup Time SDIN Hold Time	100 100	-	-	ns
T_{sdcs} T_{sdch}	SD/C Setup Time SD/C Hold Time	150 150	-	-	ns
T_{cs0s} T_{cs0h}	Chip Select Setup Time (Write) Chip Select Hold Time	150 150	-	-	ns
T_{cs0s}	Chip Select Setup before SCLK Rising Edge (Read)	0	-	-	ns



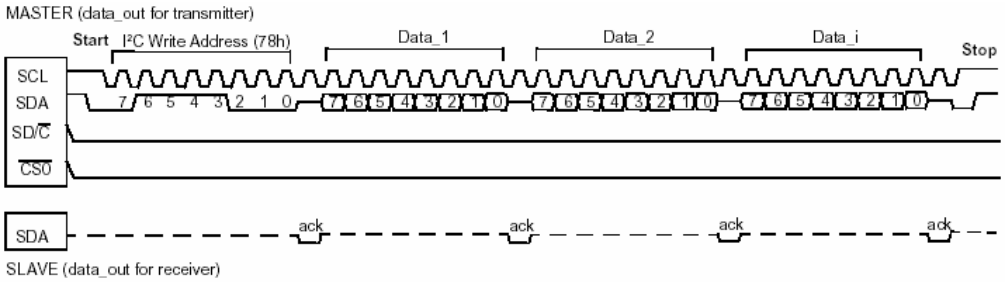
Timing Diagram for Write Mode



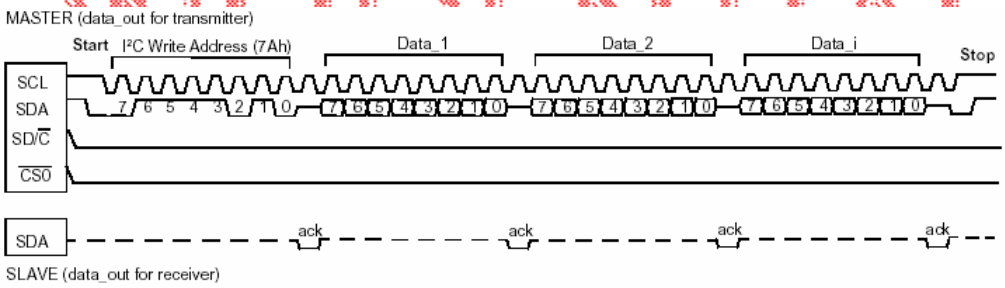
Timing Diagram for Read Mode (Register Only)

3.2.4 I²C Interface Timing Characteristics:

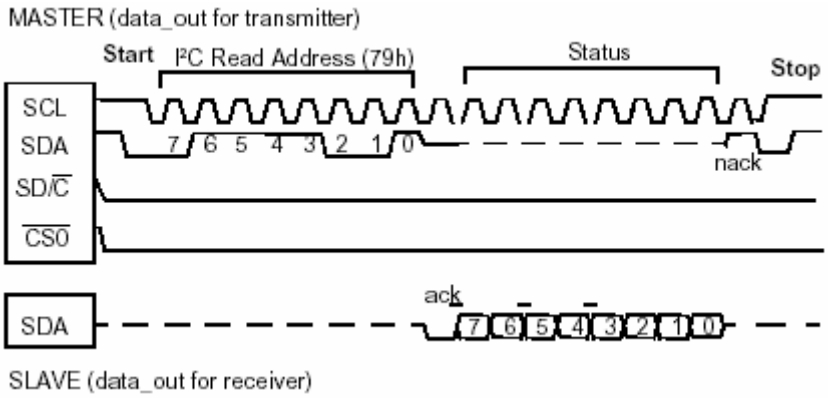
Symbol	Description	Min	Typ	Max	Unit
T_{scl_cycle}	Serial Clock Cycle Time	2.5	-	-	μs
T_{scl_low}	Write/Read Low Pulse Width	100	-	-	ns
T_{scl_high}	Select High Pulse Width	100	-	-	ns
T_{scl_rise} T_{scl_fall}	Rise Time Fall Time	-	-	15 15	ns
T_{datas} T_{datah}	Data Setup Time Data Hold Time	100 100	-	-	ns
T_{cs0s} T_{cs0h}	Chip Select Setup Time Chip Select Hold Time	120 120	-	-	ns



Timing Diagram for Write Mode (Register)



Timing Diagram for Write Mode (RAM)



Timing Diagram for Read Mode (Register Only)

3.3 Optics & Electrical Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	With Polarizer	60	80	-	cd/m^2
C.I.E. (Blue)	(x) (y)	Without Polarizer	0.12 0.22	0.16 0.26	0.20 0.30	
Dark Room Contrast	CR		-	>1:100	-	
View Angle			>160	-	-	degree

Note 3: Optical measurement taken at 1/33 duty, 66Hz Frame Rate, 7Fh Bright Setting.

3.4 General Electrical Specification

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD_D}		1.8	3.3	3.6	V
Driver Supply Voltage	V_{PP}		11	12	13	V
Operating Current for V_{DD_D}	I_{DD_D}	Note 4	-	TBD	TBD	μA
		Note 5	-	TBD	TBD	μA
Operating Current for V_{PP}	I_{PP}	Note 4	-	TBD	TBD	mA
		Note 5	-	TBD	TBD	mA
Sleep Mode Current for V_{DD_D}	$I_{DD\_D, SLEEP}$		-	TBD	-	μA
Sleep Mode Current for V_{PP}	$I_{PP, SLEEP}$		-	TBD	-	μA

Note 4: V_{DD_D} = 3.3V, V_{PP} = 12V, Frame Rate = 66Hz, Bright Setting = 7Fh, 50% Display Area Turn on.

Note 5: V_{DD_D} = 3.3V, V_{PP} = 12V, Frame Rate = 66Hz, Bright Setting = 7Fh, 100% Display Area Turn on.

4. Functional Specification

4.1. Commands

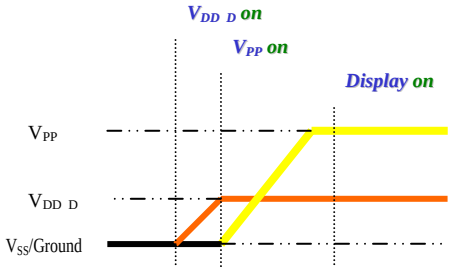
Refer to the Technical Manual for the STV8102

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

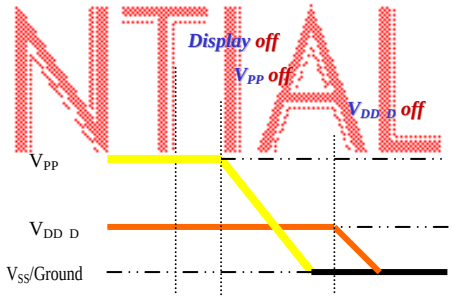
4.2.1 Power up Sequence:

1. Power up V_{DD_D}
2. Send Display off command
3. Clear Screen
4. Power up V_{PP}
5. Delay 100ms
   (when V_{DD_D} is stable)
6. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{PP}
3. Delay 100ms
   (when V_{PP} is reach 0 and panel is completely discharges)
4. Power down V_{DD_D}



4.3 Reset Circuit

The default configuration after a hardware reset is

* All the control registers are cleared.
  (Display Off, DC/DC Step-up Off, Internal Oscillator Off, Scanning Off)
* The RAM contents are unchanged.
  (on Power On: RAM contents are defined.)

The hardware reset must be applied all the power-up sequence long, until the supplies reach the minimum value.

5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	85°C, 500 hrs	The brightness should be greater than 50% of the initial brightness. The operational functions work.
Low Temperature Operation	-30°C, 500 hrs	
High Temperature Storage	90°C, 500 hrs	
Low Temperature Storage	-40°C, 500 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 500 hrs	
Thermal Shock	-40°C ⇔ 85°C, 100 cycles 30 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.
* All operation tests are conducted in all display on pattern.

5.2 Lifetime

End of lifetime is specified as 50% of initial brightness.
An estimated operating lifetime of more than 10,000 hrs at room temperature is approached by Arrhenius model's evaluation & 500 hrs @ 85°C operating.

5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15 %RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50 cm
Distance between the Panel & Eyes of the Inspector:	≥ 30 cm

Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

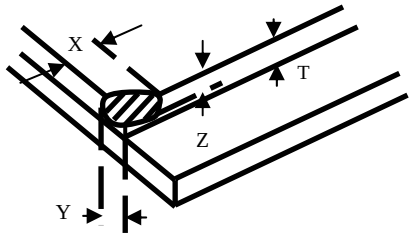
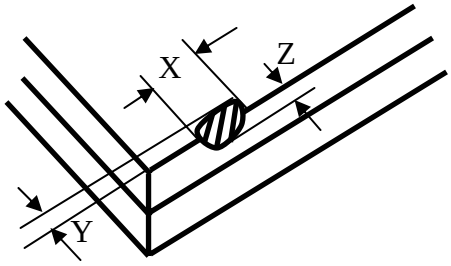
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

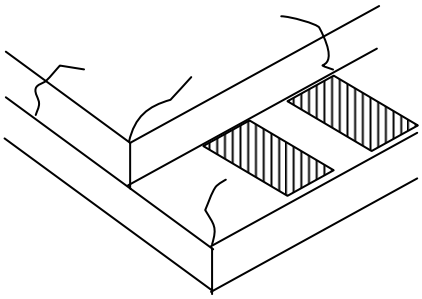
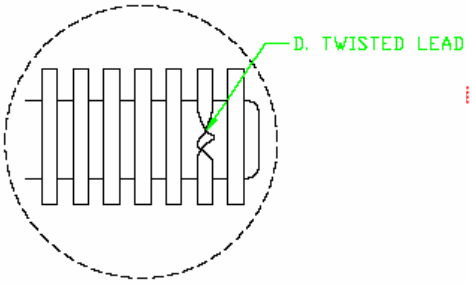
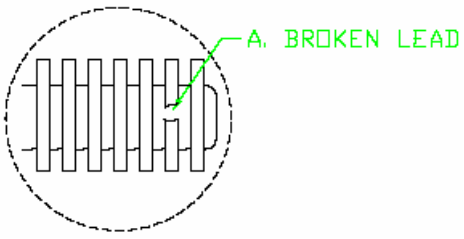
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

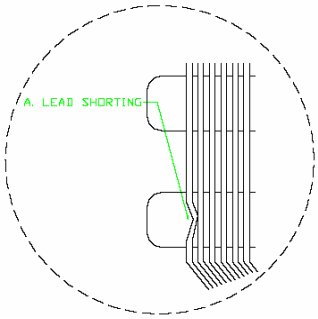
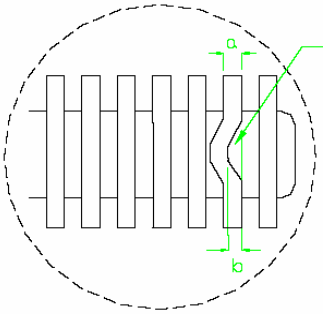
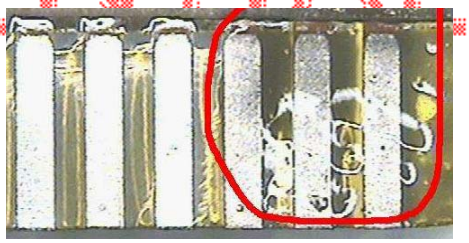
6.3.1 Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) Z ≤ T  

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Cupper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Twist	Minor	Not Allowable 
Terminal Lead Broken	Minor	Not Allowable 
Terminal Lead Prober Mark	Acceptable	Ok

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

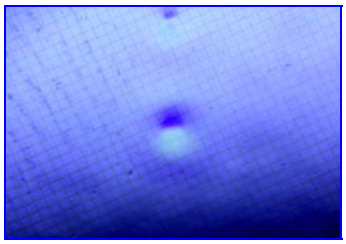
Check Item	Classification	Criteria
Terminal Lead Bent (Not Twist or Broken)	Minor	NG if any bent lead cause lead shorting. 
	Minor	NG for horizontally bent lead more than 50% of its width. 
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

6.3.2 Cosmetic Check (Display On) in Active Area

Don't tear off the protective film for only visual check purpose. Otherwise any particle or contamination of air could penetrate & attach onto the surface of polarizer in great probability. It is recommended to execute in clear room environment (class 10k) if actual in necessary.

Check Item	Classification	Criteria	
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer	
Scratches, Fiber, Line-Shape Defect ** (On Polarizer)	Minor	$W \le 0.05$ $W \le 0.1, L \le 2$ $2 < L$	Ignore $n \le 3$ $n = 0$

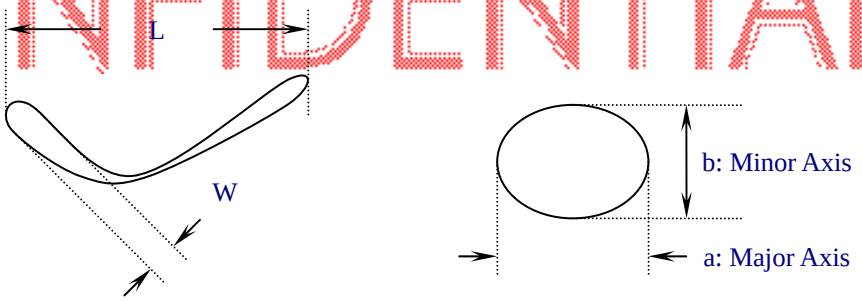
6.3.2 Cosmetic Check (Display On) in Active Area (Continued)

Check Item	Classification	Criteria
Dirt, Black Spot, Foreign Material, ** (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 < Φ ≤ 0.2 n ≤ 3 0.2 < Φ ≤ 0.25 n ≤ 1 0.25 < Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

* In displays which manifests itself has the other shadowing, ghosting or streaking.

** Distance between any 2 defects should over 10mm.

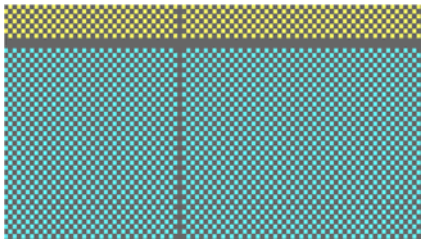
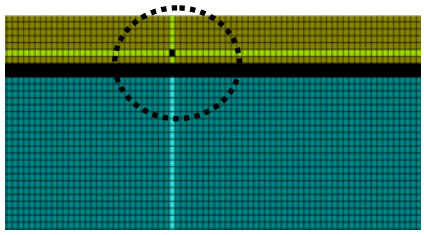
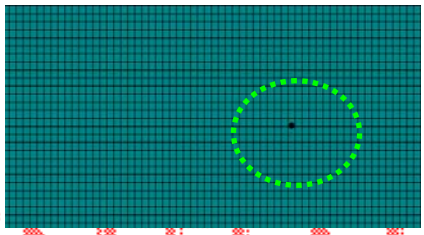
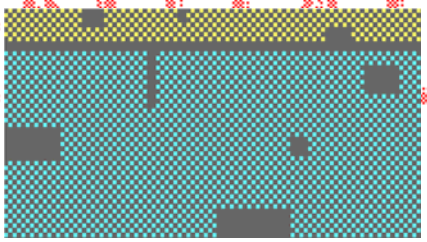
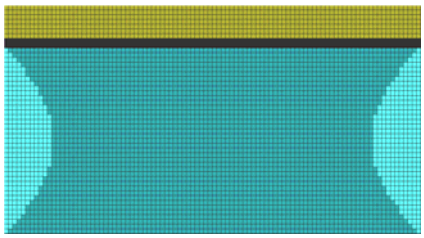
*** Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2



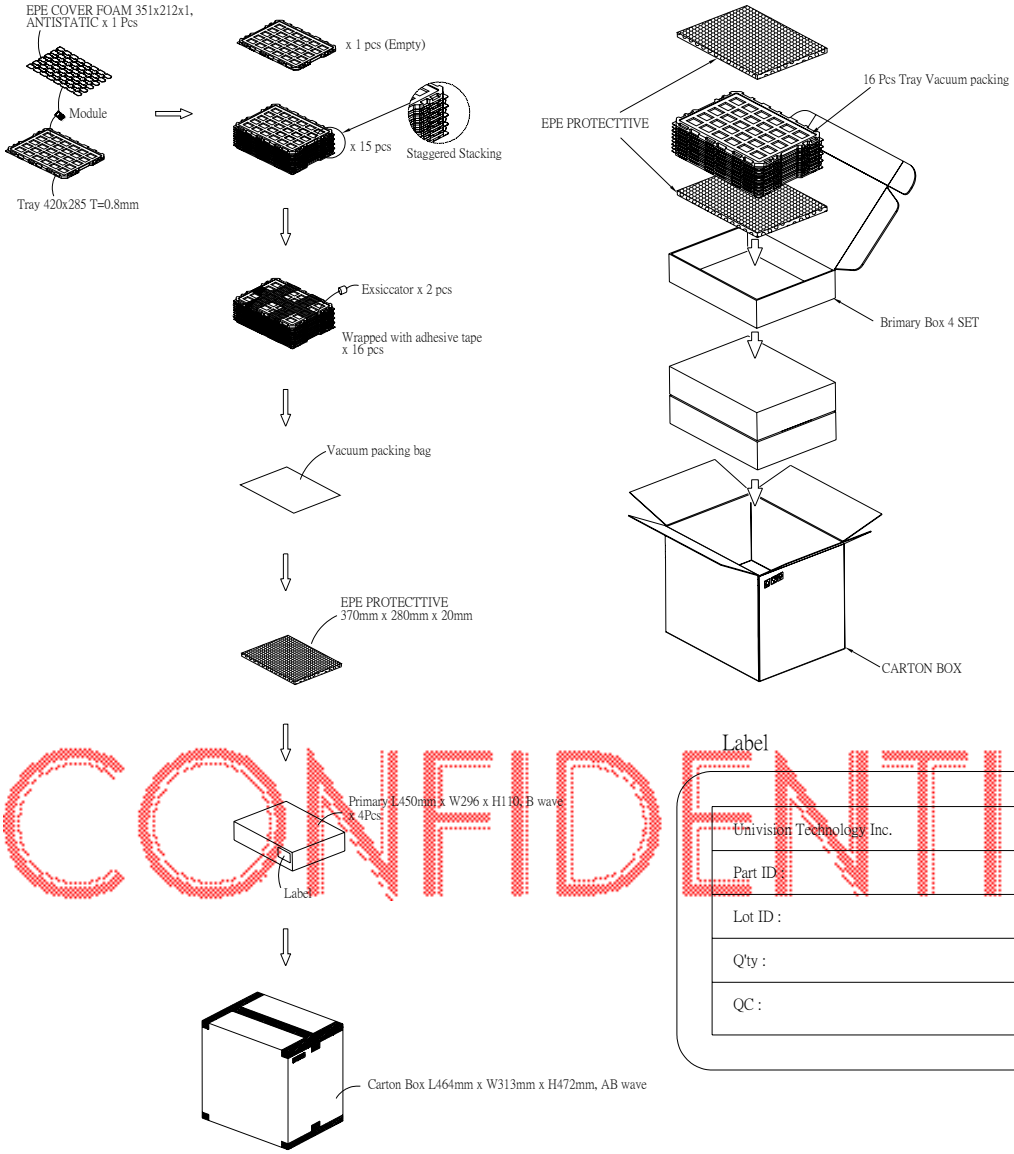
6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Flicker	Major	Not Allowable

6.3.3 Pattern Check (Display On) in Active Area (Continued)

Check Item	Classification	Criteria
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

7. Package Specifications



8. Precautions When Using These OEL Display Modules

8.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) When installing the OEL display module, be careful not to apply twisting stress or deflection stress to the OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.
7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Univision Technology Inc.)
   At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD_D). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: STV8102
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

8.4 Precautions when disposing of the OEL display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

8.5 Other Precautions

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the COF
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.