

Version : 2.0

TECHNICAL SPECIFICATION
MODEL NO : PD080SX1

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TECHNICAL SPECIFICATION
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1. Application

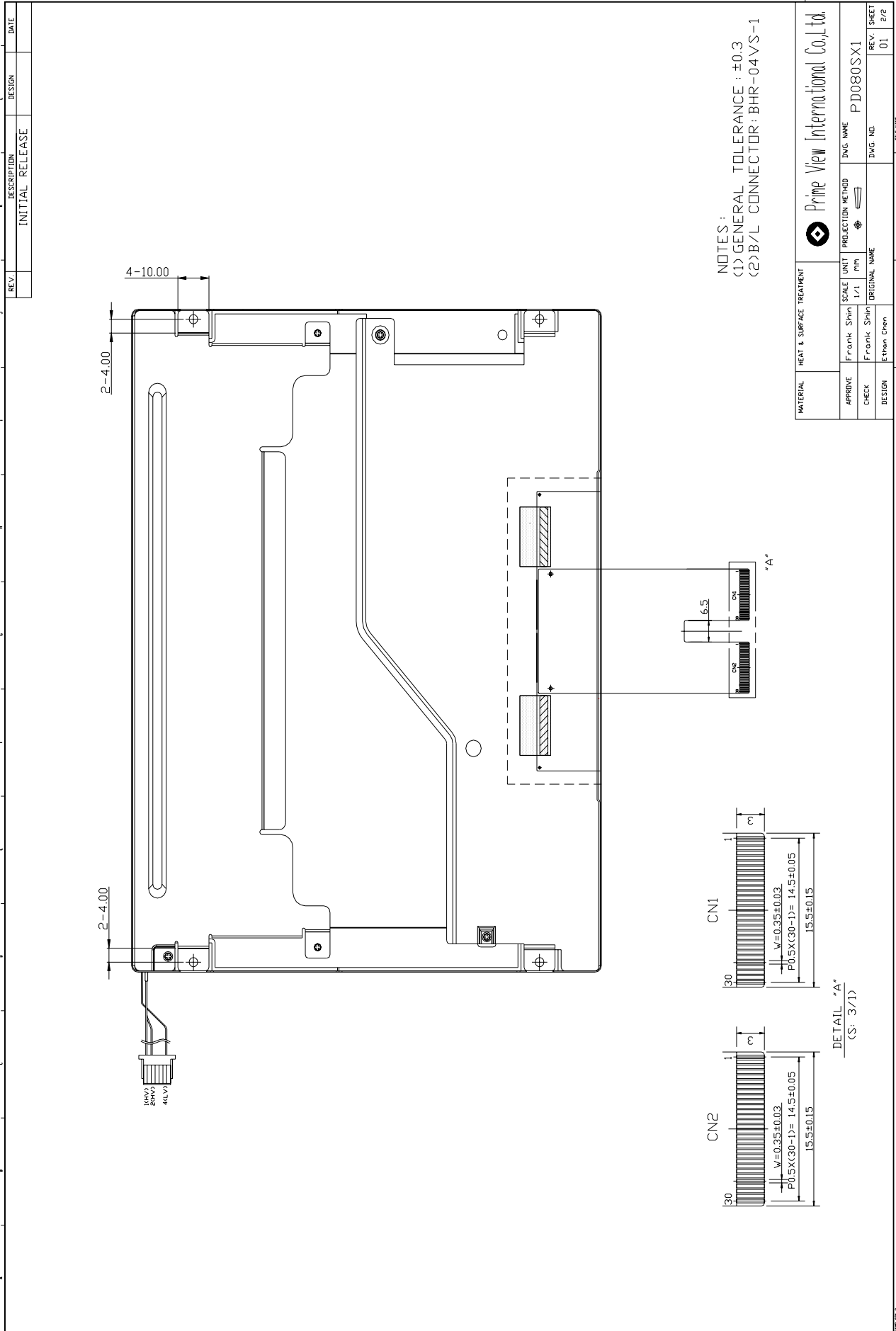
This data sheet applies to a color TFT LCD module, PD080SX1. This module applies to OA product, computer peripheral, industrial meter, image communication and multi-media. If you must use in severe reliability environment, please don't extend over PVI's reliability test conditions.

2. Features

- . Amorphous silicon TFT LCD panel with back-light unit
- . Pixel in stripe configuration
- . Slim and compact, designed for O/A application
- . Display Colors : 262,144 colors
- . Backlight driving DC/AC inverter not included in this module
- . Long Life Lamp
- . Support TTL/RSDS interface

3. Mechanical Specifications

| Parameter | Specifications | Unit |
|--------------------------------|--------------------------------------|---------|
| Screen Size | 8.0" (diagonal) | inch |
| Display Format | 800×(RGB)×600 | dot |
| Display Colors | 262,144 | |
| Active Area | 162(H)×121.5 (V) | mm |
| Pixel Pitch | 0.2025(H)×0.2025(V) | mm |
| Pixel Configuration | Stripe | |
| Outline Dimension | 200(W)×152(H)×10.5(D) (typ.) | mm |
| Weight | 322±15 | g |
| Back-light | CCFL, 2 tubes | |
| Surface treatment | Anti-Glare | |
| Display mode | Normally white | |
| Gray scale inversion direction | 6 (ref to Page 19 viewing angle) | o'clock |



5. Input / Output Terminals

5-1) TFT-LCD Panel Driving

FPC Down Connect, 30 Pins, Pitch: 0.5 mm

CN 1

| Pin No. | Symbol | I/O | Function | Remark |
|---------|---------|-----|---|-----------|
| 1 | DIO1 | I/O | Horizontal Start Pulse Signal Input or Output | Note 5-6 |
| 2 | VSS1 | I | Ground | |
| 3 | VDD1 | I | Power Supply | |
| 4 | CLK | I | Shift Clock input | Note 5-10 |
| 5 | CLKN | I | RSDS Shift Clock input | Note 5-11 |
| 6 | R/L | I | Right / Left selection | Note 5-6 |
| 7 | R0(D00) | I | Red Data (LSB) | Note 5-13 |
| 8 | R1(D01) | I | Red Data | |
| 9 | R2(D02) | I | Red Data | |
| 10 | R3(D03) | I | Red Data | |
| 11 | R4(D04) | I | Red Data | |
| 12 | R5(D05) | I | Red Data (MSB) | |
| 13 | VSS1 | I | Ground | |
| 14 | G0(D10) | I | Green Data (LSB) | Note 5-13 |
| 15 | G1(D11) | I | Green Data | |
| 16 | G2(D12) | I | Green Data | |
| 17 | G3(D13) | I | Green Data | |
| 18 | G4(D14) | I | Green Data | |
| 19 | G5(D15) | I | Green Data (MSB) | |
| 20 | VSS1 | I | Ground | |
| 21 | B0(D20) | I | Blue Data (LSB) | Note 5-13 |
| 22 | B1(D21) | I | Blue Data | |
| 23 | B2(D22) | I | Blue Data | |
| 24 | B3(D23) | I | Blue Data | |
| 25 | B4(D24) | I | Blue Data | |
| 26 | B5(D25) | I | Blue Data (MSB) | |
| 27 | LD | I | Load output signal | Note 5-7 |
| 28 | REV | I | Data invert control | Note 5-8 |
| 29 | POL | I | Polarity selection | Note 5-9 |
| 30 | DIO2 | I/O | Horizontal Start Pulse Signal Input or Output | Note 5-6 |

CN 2

| Pin No. | Symbol | I/O | Function | Remark |
|---------|---------|-----|---|-----------|
| 1 | VSS2 | I | Ground | |
| 2 | V1 | I | Gamma Voltage 1 | Note 5-14 |
| 3 | V2 | I | Gamma Voltage 2 | |
| 4 | V3 | I | Gamma Voltage 3 | |
| 5 | V4 | I | Gamma Voltage 4 | |
| 6 | V5 | I | Gamma Voltage 5 | |
| 7 | V6 | I | Gamma Voltage 6 | |
| 8 | V7 | I | Gamma Voltage 7 | |
| 9 | VSS2 | I | Ground | |
| 10 | V8 | I | Gamma Voltage 8 | Note 5-14 |
| 11 | V9 | I | Gamma Voltage 9 | |
| 12 | V10 | I | Gamma Voltage 10 | |
| 13 | V11 | I | Gamma Voltage 11 | |
| 14 | V12 | I | Gamma Voltage 12 | |
| 15 | V13 | I | Gamma Voltage 13 | |
| 16 | V14 | I | Gamma Voltage 14 | |
| 17 | VSS2 | I | Ground | |
| 18 | VDD2 | I | Voltage for analog circuit | Note 5-14 |
| 19 | VCOM | I | Common Voltage | |
| 20 | TTLRSDS | I | TTL / RSDS Input mode Selection | Note 5-12 |
| 21 | OE | I | Output Enable | Note 5-5 |
| 22 | U/D | I | Up / Down Selection | Note 5-3 |
| 23 | CKV | I | Vertical Shift Clock | Note 5-4 |
| 24 | STVU | I/O | Vertical Shift Pulse Signal Input or Output | Note 5-3 |
| 25 | STVD | I/O | Vertical Shift Pulse Signal Input or Output | |
| 26 | VGG | I | Gate On Voltage | Note 5-2 |
| 27 | GND | I | Ground | |
| 28 | VCC | I | Voltage for logic circuit | |
| 29 | GND | I | Ground | |
| 30 | VEE | I | Gate Off Voltage | Note 5-1 |

Note 5-1: Gate off voltage, $V_{EE}=-5.5V$

Note 5-2: Gate on voltage, $V_{GG}=15.5V$

Note 5-3: Select up or down shift

| U/D | STVU | STVD | Shift |
|-----|-------|-------|------------|
| 1 | Hi-Z | Input | Down to Up |
| 0 | Input | Hi-Z | Up to Down |

Note 5-4: Gate driver shift clock

Note 5-5: When OE is connected to high “1”, the driver outputs are disabled (Gate output = V_{EE}).
Under this condition, the operation of registers will not be affected.

Note 5-6: Select left or right shift

| R/L | DIO1 | DIO2 | Shift |
|-----|-------|-------|---------------|
| 1 | Input | Hi-Z | Left to right |
| 0 | Hi-Z | Input | Right to left |

Note 5-7: Latch the polarity of outputs and switch the new data to outputs. At the rising edge (LD), latch the “POL” signal to control the polarity of the outputs.

Note 5-8: Control whether the Data R0~G5 are inverted or not. (PVI suggests connecting to GND)
When “REV=1”, these data will be inverted. Ex: “00” ”3F”, “07” ”38”, “15” ”2A”

Note 5-9: Polarity selector for dot-inversion control. Available at the rising edge of LD.

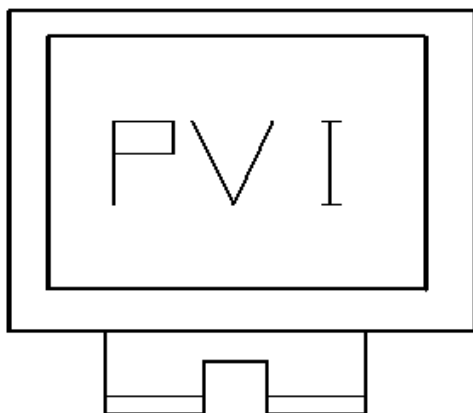
When POL=1: Even outputs range from V1~V7, and Odd outputs range from V8~V14;
When POL=0: Even outputs range from V8~V14, and Odd outputs range from V1~V7.

Note 5-10: Clock signal. When RSDS input mode, CLK is used as CLKP input pin.

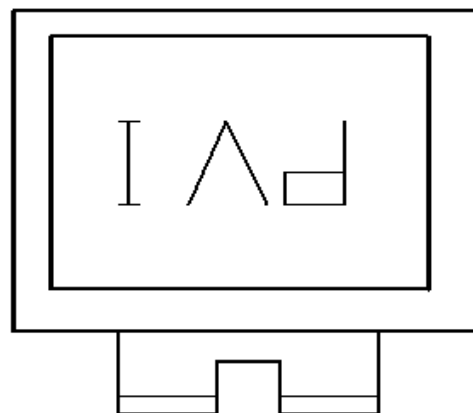
Note 5-11: The RSDS clock input pairs generate the internal shift clock through the comparison between CLKP and CLKN. When TTL mode, connect to GND.

Note 5-12: TTLRSDS=H: RSDS data input
TTLRSDS=L or open: TTL data input

U/D CN2(PIN22)=0 R/L CN1(PIN6)=1



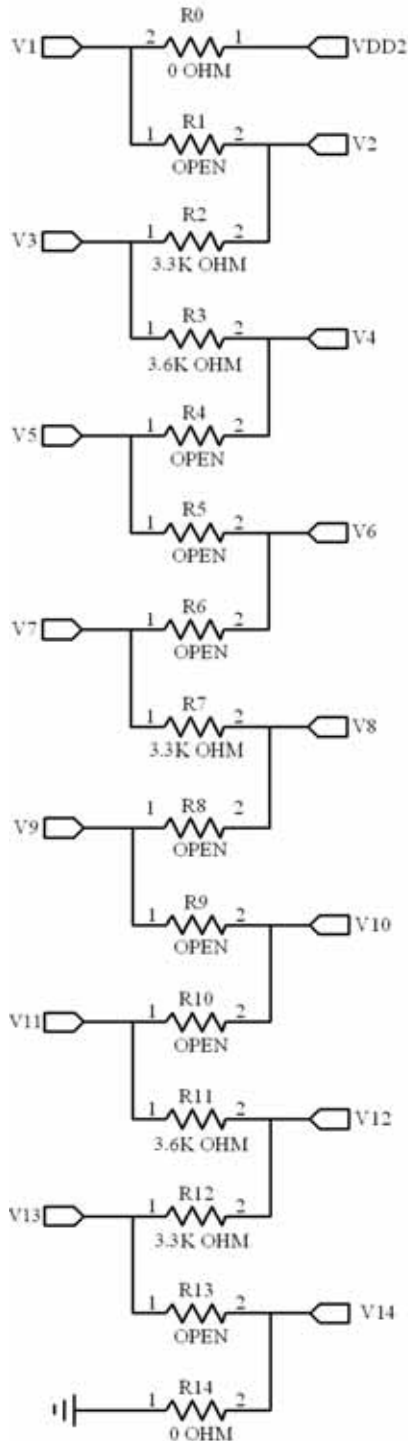
U/D CN2(PIN22)=1 R/L CN1(PIN6):



Note 5-13:

| Pin name | RSDS input mode TTLRSDS = H | TTL input mode TTLRSDS = L |
|-------------|--------------------------------|-------------------------------|
| D04,D02,D00 | D0[2:0]N | D04,D02,D00 |
| D05,D03,D01 | D0[2:0]P | D05,D03,D01 |
| D14,D12,D10 | D1[2:0]N | D14,D12,D10 |
| D15,D13,D11 | D1[2:0]P | D15,D13,D11 |
| D24,D22,D20 | D2[2:0]N | D24,D22,D20 |
| D25,D23,D21 | D2[2:0]P | D25,D23,D21 |

Note 5-14: Typical Application Circuit (When $V_{DD2} = 7.7V$)



6. Absolute Maximum Ratings:
 $V_{SS1}=V_{SS2}=GND=0V, T_a=25$

| Parameters | Symbol | MIN. | MAX. | Unit | Remark |
|----------------|-----------------|------|------|------|--------|
| Supply Voltage | V_{DD1} | -0.5 | 5.0 | V | |
| | V_{CC} | -0.3 | 6.0 | V | |
| | V_{DD2} | -0.5 | 12.0 | V | |
| | V_{GG} | -0.3 | 40.0 | V | |
| | $V_{GG}-V_{EE}$ | -0.3 | 40.0 | V | |
| | V_{EE} | -20 | 0.3 | V | |

7. Electrical Characteristics
7-1) Recommended Operating Conditions :
 $V_{SS1}=V_{SS2}=GND=0V, T_a=25$

| Item | Symbol | Min. | Typ. | Max. | Unit | Remark |
|----------------------------------|-----------|--------------|------|--------------|------|--------|
| Supply Voltage for Source Driver | V_{DD1} | - | 3.3 | - | V | |
| | V_{DD2} | - | 7.7 | - | V | |
| Supply Voltage for Gate Driver | V_{GG} | - | 15.5 | - | V | |
| | V_{EE} | - | -5.5 | - | V | |
| | V_{CC} | - | 3.3 | - | V | |
| V_{com} Voltage | V_{com} | - | 3.3 | - | V | |
| Digital Input Voltage | V_{IH} | $0.7 V_{CC}$ | - | V_{CC} | V | |
| | V_{IL} | 0 | - | $0.3 V_{CC}$ | V | |

7-2) Recommended Driving Condition for Back Light
 $T_a=25$

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---|--------|------|------|------|------|-----------|
| Lamp Voltage | V_L | 460 | 510 | 580 | V | $I_L=5mA$ |
| Lamp Current | I_L | 3 | 5 | 8 | mA | Note 7-1 |
| Lamp Frequency | P_L | 25 | 40 | 80 | KHz | Note 7-2 |
| Starting Voltage (25) (Reference Value) | V_s | - | - | 960 | Vrms | Note 7-3 |
| Starting Voltage (0) (Reference Value) | V_s | - | - | 1030 | Vrms | Note 7-3 |

Note 7-1: In order to satisfy the quality of B/L, no matter use what kind of inverter, the output lamp current must between Min. and Max. to avoid the abnormal display image caused by B/L.

Note 7-2: The waveform of lamp driving voltage should be as closed to a perfect sine wave
As possible.

Note 7-3: The “Starting voltage” means the minimum voltage of inverter to turn on the CCFL. and it should be applied to the lamp for more than 1 second start up. Otherwise the lamp may not be turned on.

7-3) Power Consumption

| Parameter | Symbol | Condition | Typ. | Max. | Unit | Remark |
|--|-----------|-----------------|--------|--------|------|----------|
| Supply Current for Gate Driver (Hi level) | I_{GG} | $V_{GG}= 15.5V$ | 0.21 | 0.26 | mA | |
| Supply Current for Gate Driver (Low level) | I_{EE} | $V_{EE}= -5.5V$ | 0.22 | 0.27 | mA | |
| Supply Current for Source Driver (Digital) | I_{DD1} | $V_{DD1}= 3.3V$ | 0.22 | 0.27 | mA | |
| Supply Current for Source Driver (Analog) | I_{DD2} | $V_{DD2}= 7.7V$ | 40.49 | 50.61 | mA | |
| Supply Current for Gate Driver (Digital) | I_{CC} | $V_{CC}= 3.3V$ | 0.32 | 0.39 | mA | |
| LCD Panel Power Consumption | - | - | 318.02 | 397.39 | mW | Note 7-4 |
| Backlight Lamp Power Consumption | PL | - | 5.1 | 8 | W | Note 7-5 |

Note 7-4: The power consumption for backlight is not included.

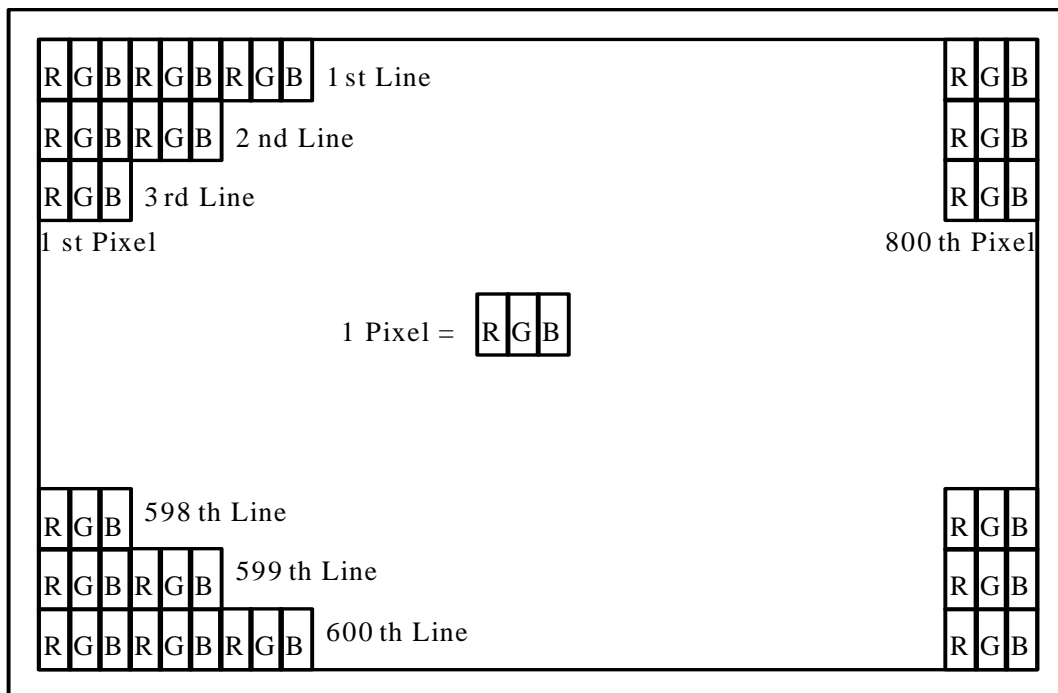
Note 7-5: Back light lamp power consumption is calculated by $I_L \times V_L$.

7-4) Backlight driving

Connector type : “BHR-04VS-1” of Japan Solder less Terminal MFG Co. LTD

| PIN NO. | Symbol | Description | Remark |
|---------|--------|----------------------|--------|
| 1 | VL1 | Input Voltage (High) | |
| 2 | VL2 | Input Voltage (High) | |
| 3 | NC | | |
| 4 | VL4 | Input Voltage (Low) | |

8. Pixel Arrangement

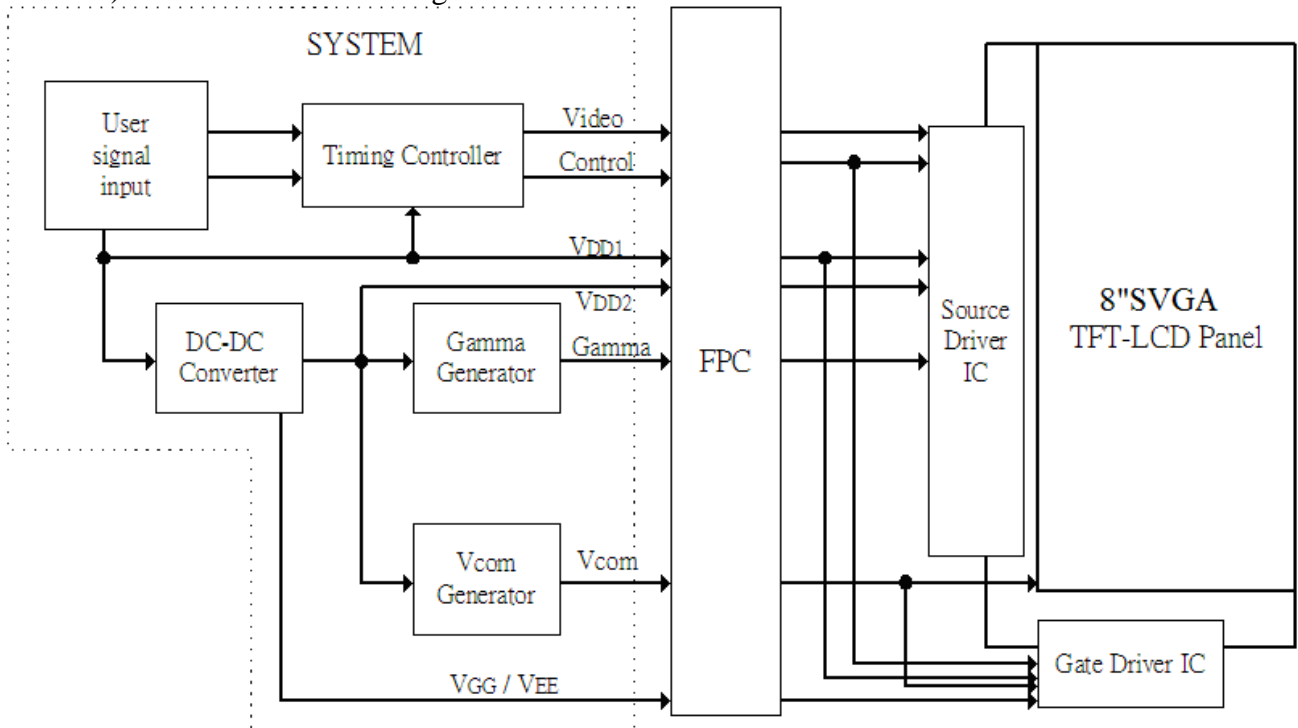


9. Display Color and Gray Scale Reference

| Color | | Input Color Data | | | | | | | | | | | | | | | | | |
|--------------|------------|------------------|----|----|----|----|----|-------|----|----|----|----|----|------|----|----|----|----|----|
| | | Red | | | | | | Green | | | | | | Blue | | | | | |
| | | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 |
| Basic Colors | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red (63) | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green (63) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Blue (63) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Cyan | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Magenta | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Yellow | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | White | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Red | Red (00) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red (01) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red (02) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Darker | | | | | | | | | | | | | | | | | | |
| | Brighter | | | | | | | | | | | | | | | | | | |
| | Red (61) | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red (62) | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red (63) | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Green | Green (00) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green (01) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green (02) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Darker | | | | | | | | | | | | | | | | | | |
| | Brighter | | | | | | | | | | | | | | | | | | |
| | Green (61) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green (62) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green (63) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Blue | Blue (00) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Blue (01) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | Blue (02) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | Darker | | | | | | | | | | | | | | | | | | |
| | Brighter | | | | | | | | | | | | | | | | | | |
| | Blue (61) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| | Blue (62) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| | Blue (63) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

10. Block Diagram

10-1) TFT-module Block Diagram



11. Interface Timing

11-1) Timing Parameters

AC Electrical Characteristics ($V_{CC}=V_{DD1}=3.3V$, $V_{DD2}=7.7V$, $GND=V_{SS1}=V_{SS2}=0V$, $T_a=25$)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|--------------------------------|-----------------------|-----------------------|------|-----------------------|-----------------|------------------------------|
| CLK Frequency | Fclk | - | 40 | 45 | MHz | |
| CLK Pulse Width | Tcw | 22 | - | - | ns | |
| Data Set-up Time | Tsu | 4 | - | - | ns | |
| Data Hold Time | Thd | 2 | - | - | ns | |
| Propagation Delay of DIO2/1 | Tphl | 6 | 10 | 15 | ns | |
| Time That The Last Data to LD | Tld | 1 | - | - | Tcw | |
| Pulse width of LD | Twld | 2 | - | - | Tcw | |
| Time That LD to DIO1/2 | Tlds | 5 | - | - | Tcw | |
| POL Set-up Time | Tpsu | 6 | - | - | ns | |
| POL Hold Time | Tphd | 6 | - | - | ns | |
| OE Pulse Width | T _{OE} V | 1 | - | - | μs | |
| CKV Pulse Width | T _{CKV} | 500 | - | - | ns | |
| STV Set-up Time | T _{SUV} | 400 | - | - | ns | |
| STV Hold Time | T _H DV | 400 | - | - | ns | |
| Horizontal Display Period | T _{HDP} | 800 | 800 | 800 | Tcw | |
| Horizontal Period Timing Range | T _{HP} | 920 | 1056 | 1064 | Tcw | |
| Horizontal Lines Per Field | T _V | 604 | 628 | 800 | T _{HP} | |
| Vertical Display Timing Range | T _{DV} | 600 | 600 | 600 | T _{HP} | |
| RSDS Low level Input Voltage | V _l rsds | - | -200 | -100 | mV | D2[2:0]P,D2[2:0]N, CLKP,CLKN |
| RSDS High level Input Voltage | V _h rsds | 100 | 200 | - | mV | D2[2:0]P,D2[2:0]N, CLKP,CLKN |
| RSDS reference Voltage | V _{com} rsds | V _{SS1} +0.1 | 1.2 | V _{DD1} -1.2 | V | D2[2:0]P,D2[2:0]N, CLKP,CLKN |

11-2) Timing Diagram

- $V_{cmrsds} = (V_{CLKP} + V_{CLKN}) / 2$ or $V_{cmrsds} = (V_{DxxP} + V_{DxxN}) / 2$
- $V_{diffrsds} = V_{CLKP} - V_{CLKN}$ or $V_{diffrsds} = V_{DxxP} - V_{DxxN}$

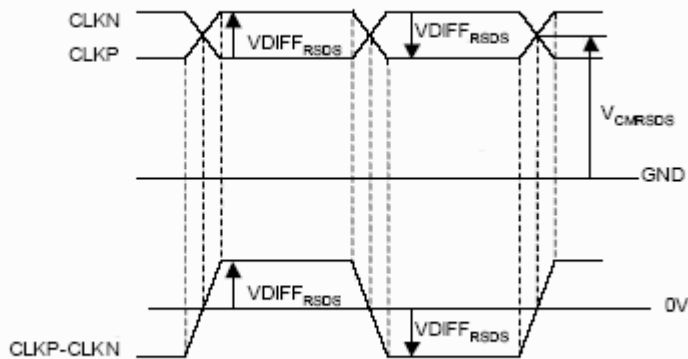


Figure11-1 RSDS clock

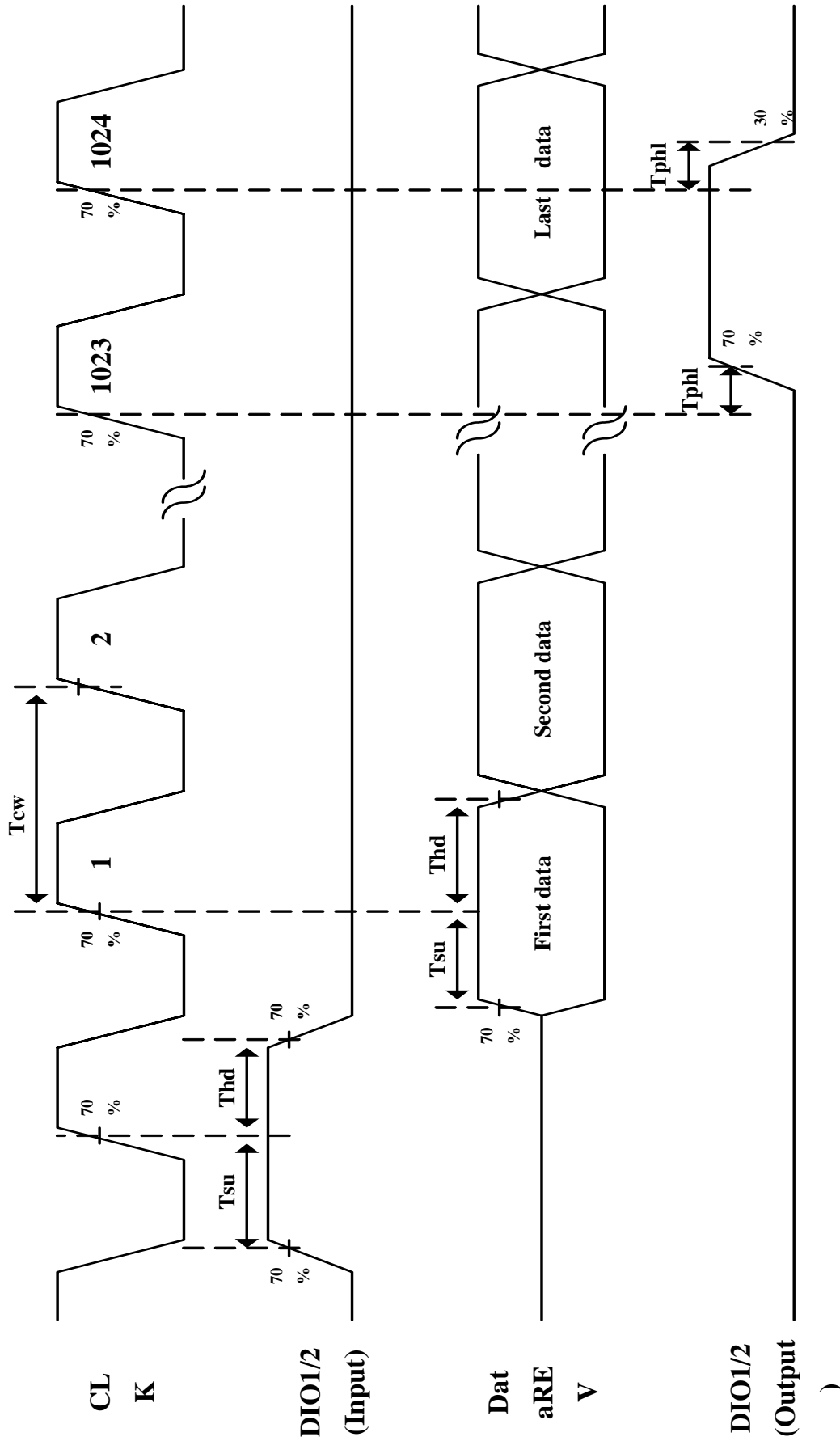


Fig. 11-2 Horizontal timing-TTL(1)

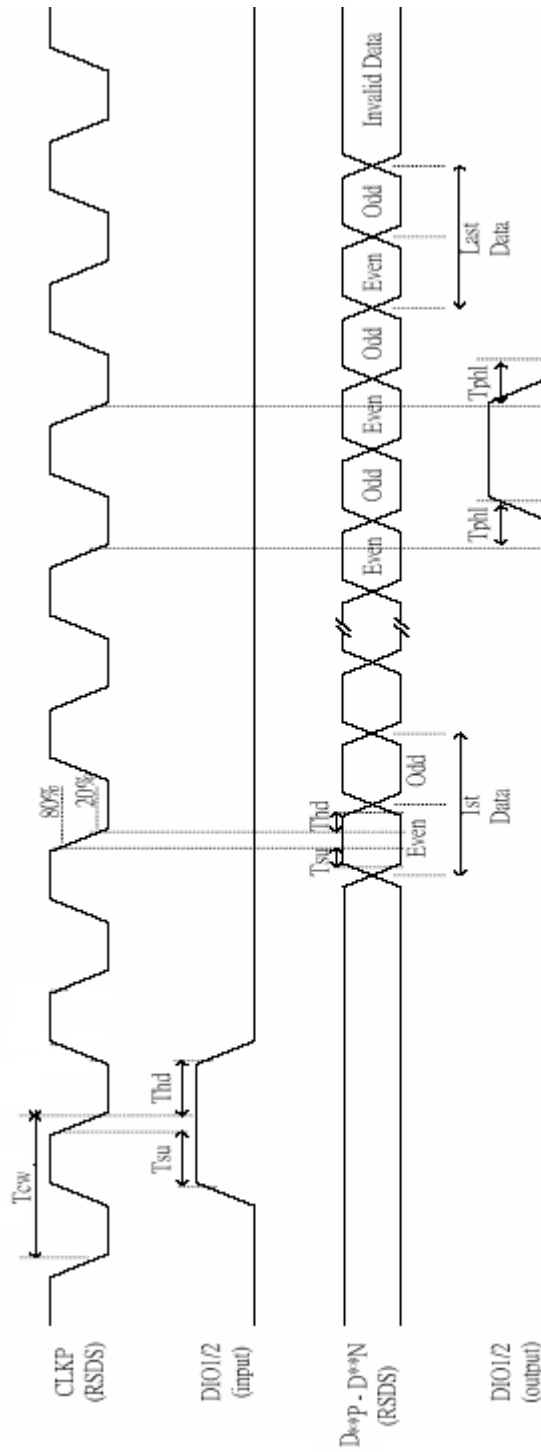


Figure 11-2 Horizontal timing-RSDS(2)

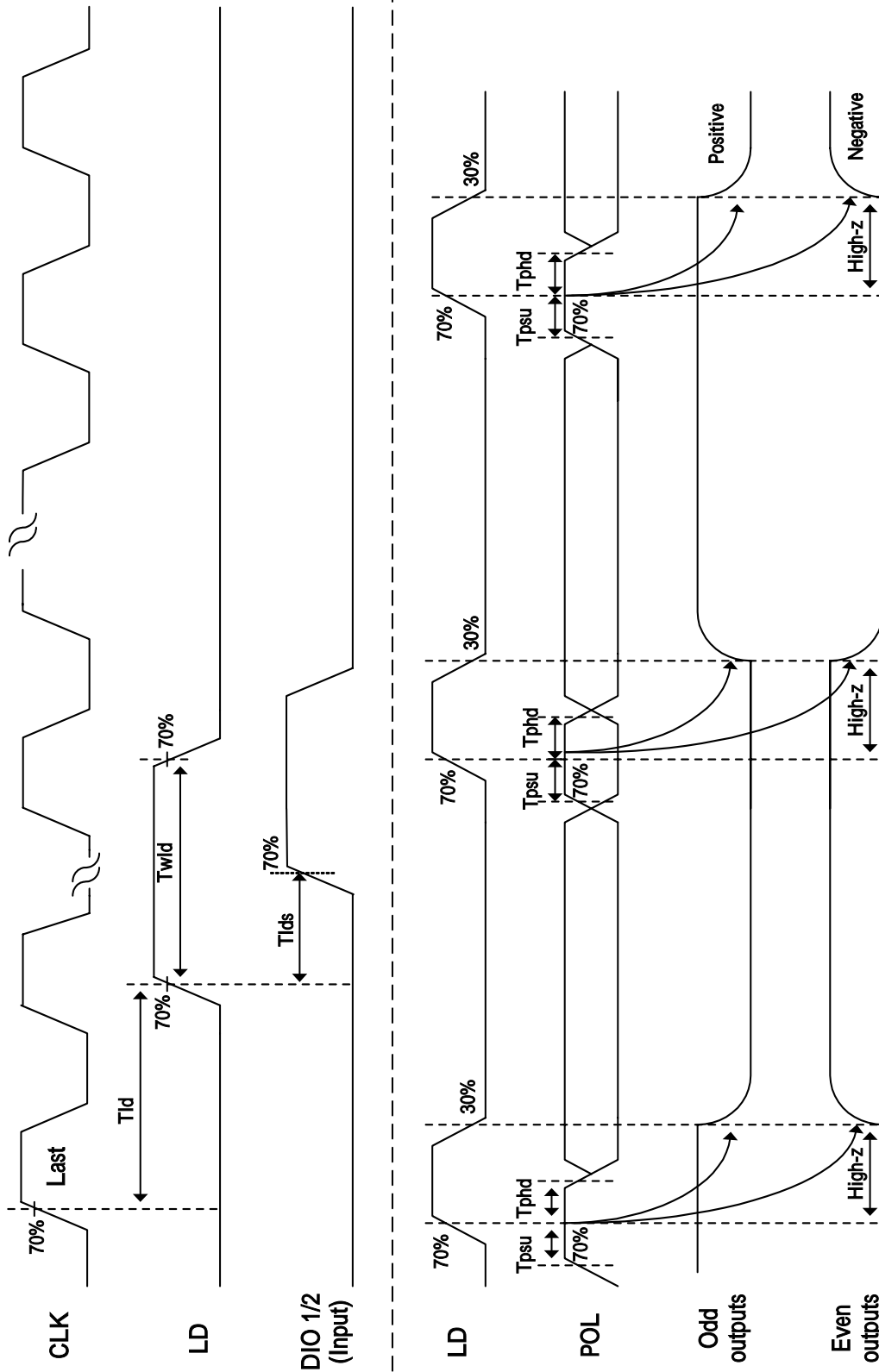


Fig. 11-3 Horizontal timing

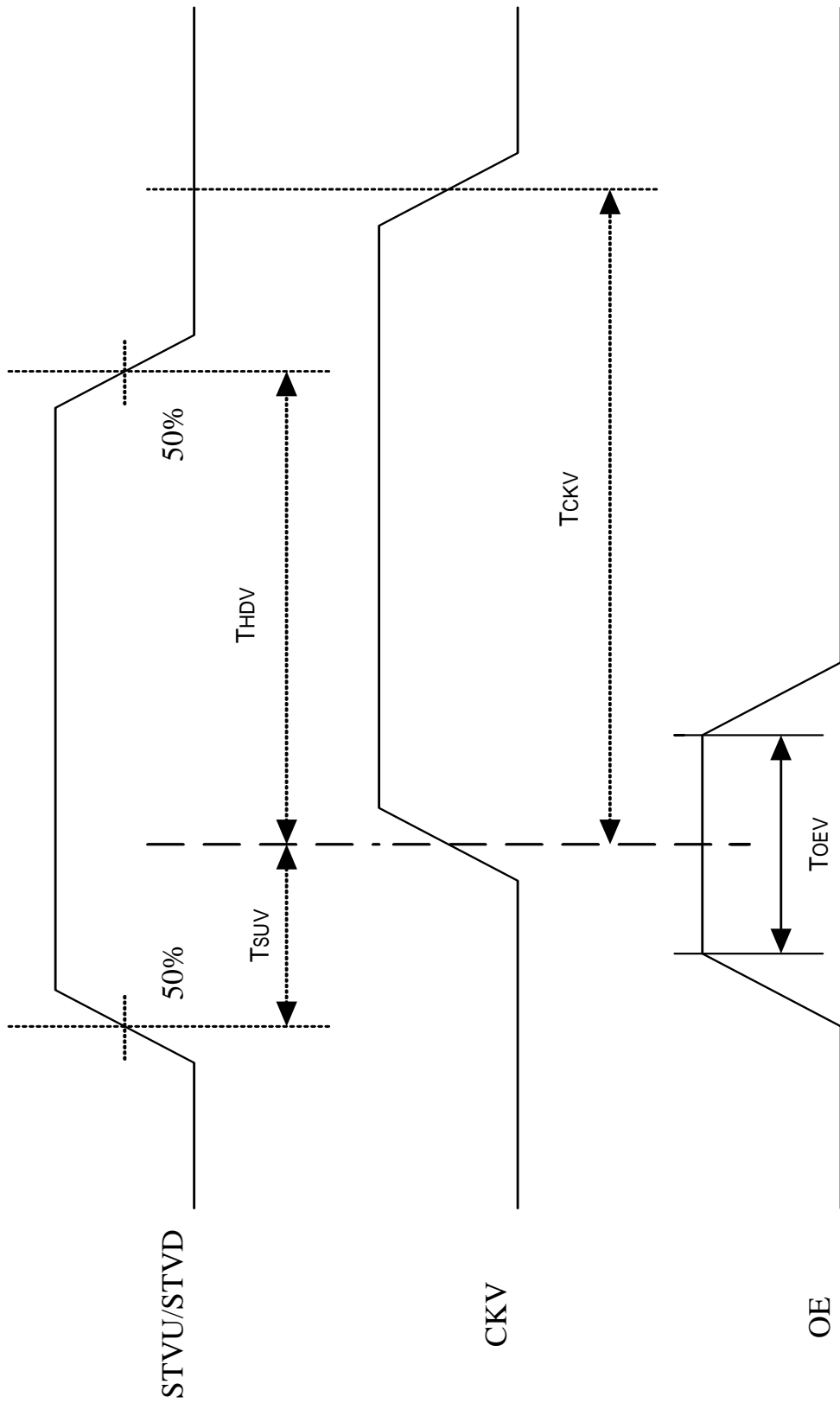


Fig. 11-4 Vertical shift clock timing

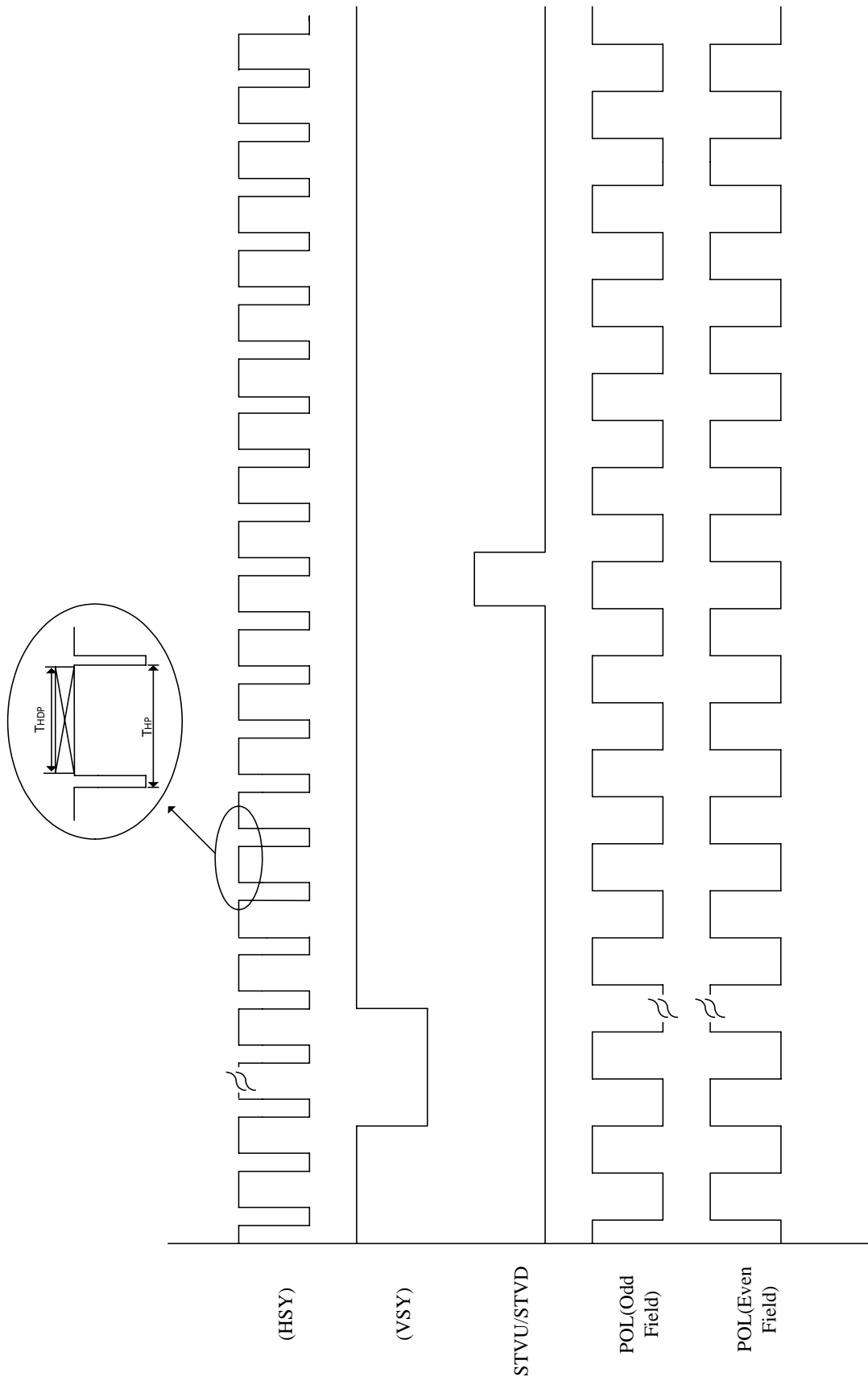
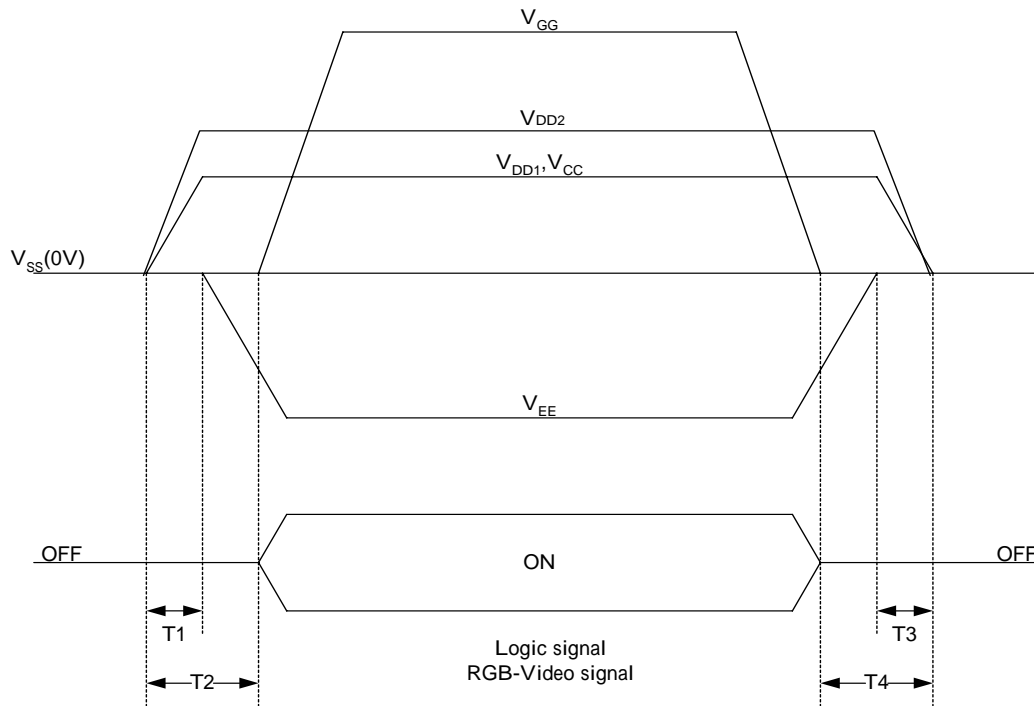


Fig. 11-5 Vertical timing

12. Power On Sequence



1. 10ms $T_1 < T_2$
2. 0ms $< T_3$ T_4 10ms

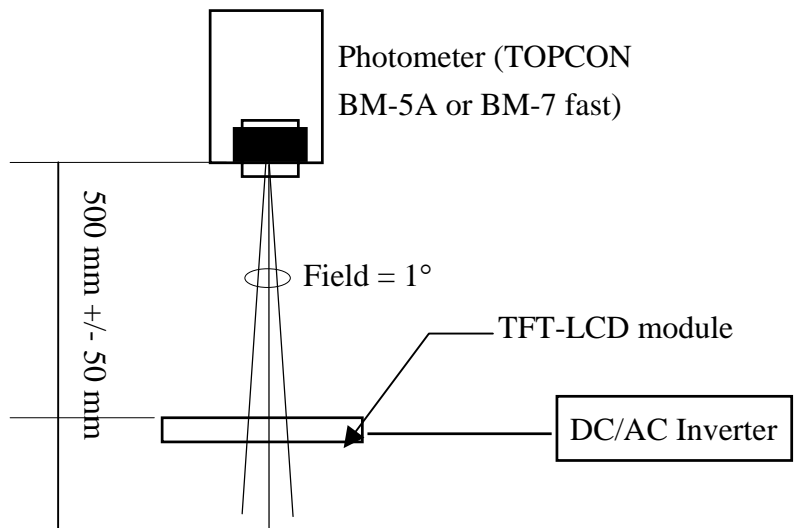
13. Optical Characteristics

13-1) Specification:

$T_a = 25$

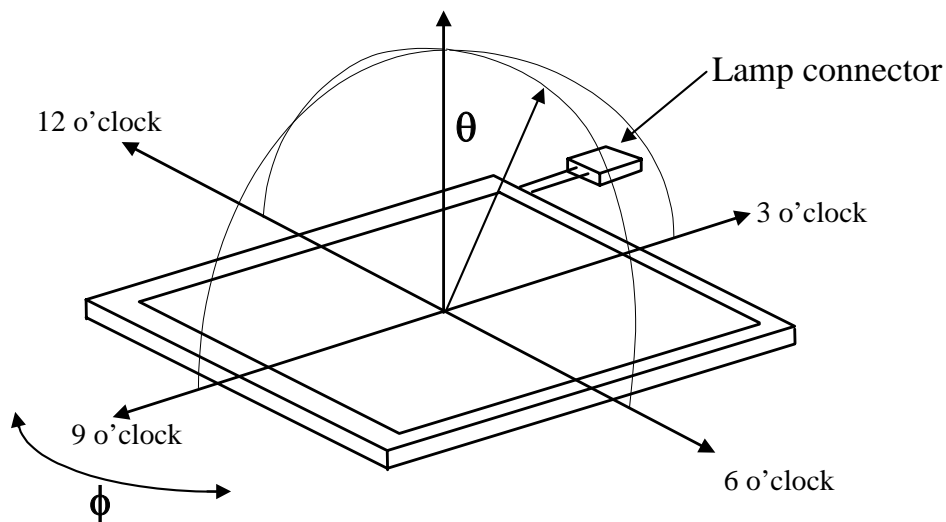
| Parameter | | Symbol | Condition | MIN. | TYP. | MAX. | Unit | Remarks |
|----------------------|------------|----------------|-----------------------|-------|------|------|----------|--------------|
| Viewing Angle | Horizontal | | $CR \geq 10$ | 55 | 60 | - | deg | Note 13-1 |
| | Vertical | (to 12 'clock) | | 30 | 35 | - | deg | |
| | | (to 6 o'clock) | | 45 | 50 | - | deg | |
| Contrast Ratio | | CR | Optimum direction | 200 | 400 | - | - | Note 13-2 |
| Response time | Rise | T_r | $=0^\circ$ | - | 15 | 30 | ms | Note 13-4 |
| | Fall | T_f | $=0^\circ$ | - | 25 | 50 | ms | |
| Luminance | | L | $=0^\circ / =0^\circ$ | 390 | 420 | - | cd/m^2 | Note 13-3 |
| Luminance Uniformity | | U | - | 75 | 80 | - | % | Note 13-5 |
| White Chromaticity | | x | $=0^\circ / =0^\circ$ | 0.29 | 0.32 | 0.35 | - | |
| | | y | $=0^\circ / =0^\circ$ | 0.32 | 0.35 | 0.38 | - | |
| Lamp Life Time | | - | 25 | 50000 | - | - | hrs | $I_{FL}=5mA$ |
| Cross Talk Ratio | | CTK | - | - | - | 3.5 | % | Note 13-6 |

All the optical measurement shall be executed 30 minutes after backlight being turn-on.
 The optical characteristics shall be measured in dark room (ambient illumination on panel surface less than 1 Lux). The measuring configuration shows as following figure.



Optical characteristics measuring configuration

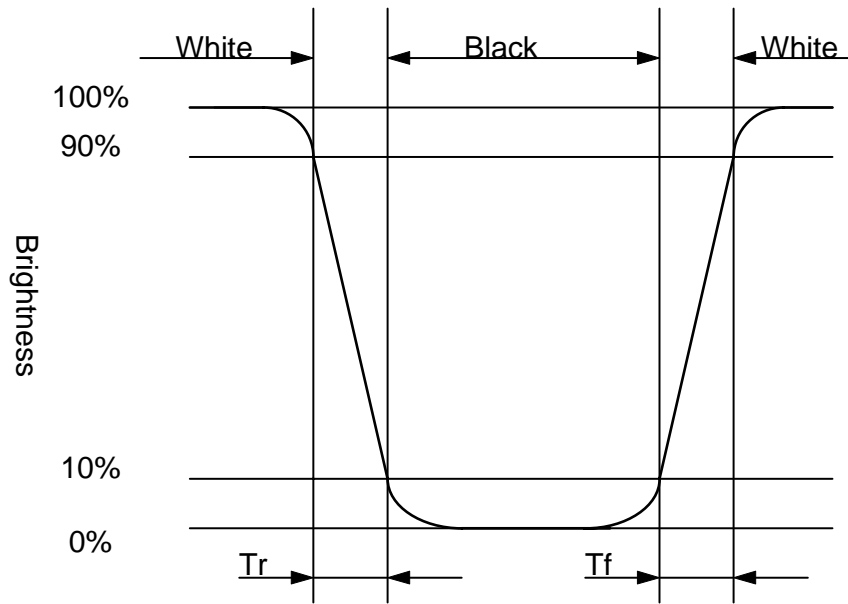
Note 13-1: The definitions of viewing angles are as follow



Note 13-2 : The definition of contrast ratio $CR = \frac{\text{Luminance at gray level 63}}{\text{Luminance at gray level 0}}$

Note 13-3: Topcon BM-5A or BM-7 fast luminance meter 1° field of view is used in the testing (after 30 minutes' operation). The typical luminance value is measured at lamp current 5.0 mA.

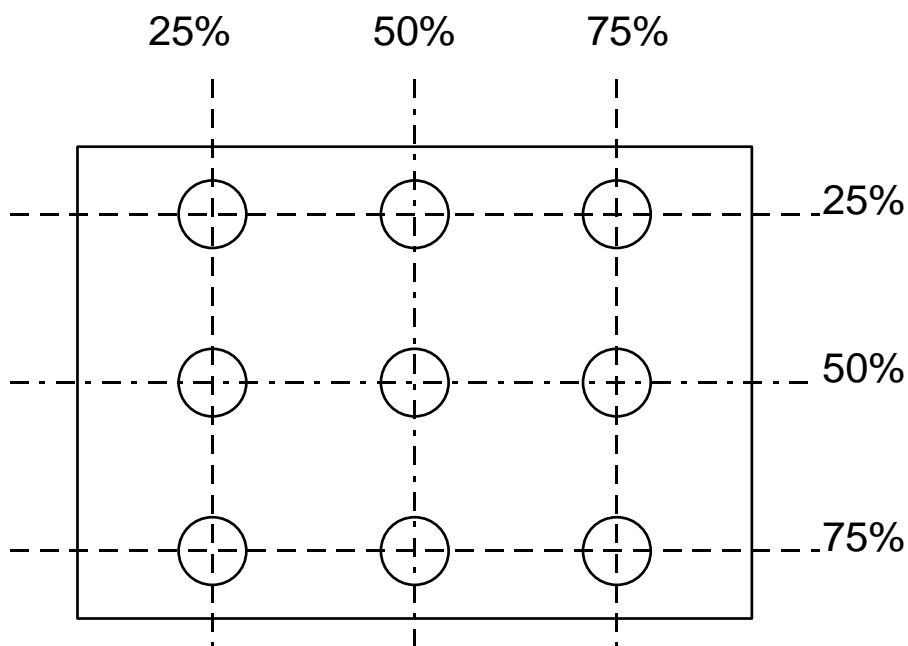
Note 13-4: Definition of Response Time T_r and T_f :



Note 13-5: The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

- Luminance meter : BM-5A or BM-7 fast(TOPCON)
- Measurement distance : 500 mm +/- 50 mm
- Ambient illumination : < 1 Lux
- Measuring direction : Perpendicular to the surface of module
- The test pattern is white (Gray Level 63).



Note 13-6: Cross Talk (CTK) = $\frac{|YA-YB|}{YA} \times 100\%$

YA: Brightness of Pattern A

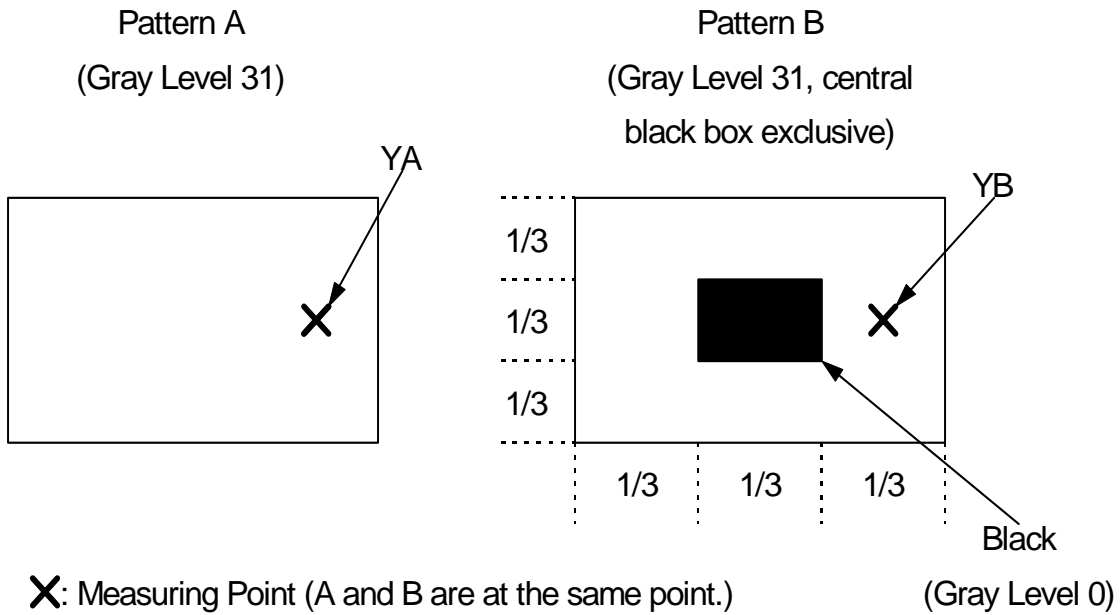
YB: Brightness of Pattern B

Luminance meter : BM 5A (TOPCON)

Measurement distance : 500 mm +/- 50 mm

Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module



14. Handling Cautions

14-1) Mounting of module

- a) Please power off the module when you connect the input/output connector.
- b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.
 - 1.The noise from the backlight unit will increase.
 - 2.The output from inverter circuit will be unstable.
 - 3.In some cases a part of module will heat.
- c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

14-2) Precautions in mounting

- a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
- b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

14-3) Adjusting module

- a) Adjusting volumes on the rear face of the module have been set optimally before shipment.
- b) Therefore, do not change any adjusted values. If adjusted values are changed, the Specifications described may not be satisfied.

14-4) Others

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.
- f) Please adjust the voltage of common electrode as material of attachment by 1 module.

15. Reliability Test

| No | Test Item | Test Condition |
|----|---|---|
| 1 | High Temperature Storage Test | Ta = +80 , 240 hrs |
| 2 | Low Temperature Storage Test | Ta = -20 , 240 hrs |
| 3 | High Temperature Operation Test | Ta = +80 , 240 hrs |
| 4 | Low Temperature Operation Test | Ta = -20 , 240 hrs |
| 5 | High Temperature & High Humidity Operation Test | Ta = +60 , 90%RH, 240 hrs (No Condensation) |
| 6 | Thermal Cycling Test (non-operating) | -20 \leftrightarrow +80 , 100 Cycles 30 min 30 min |
| 7 | Vibration Test (non-operating) | Frequency : 10 ~ 57 Hz, Amplitude : 0.15 mm 58~500Hz, 1G Sweep time : 11 min Test Period : 3 hrs (1 hr for each direction of X, Y, Z) |
| 8 | Shock Test (non-operating) | 80G, 6ms, X,Y, Z 1 times for each direction |
| 9 | Electrostatic Discharge Test (non-operating) | 200pF , 0 \pm 200V 1 time / each terminal |

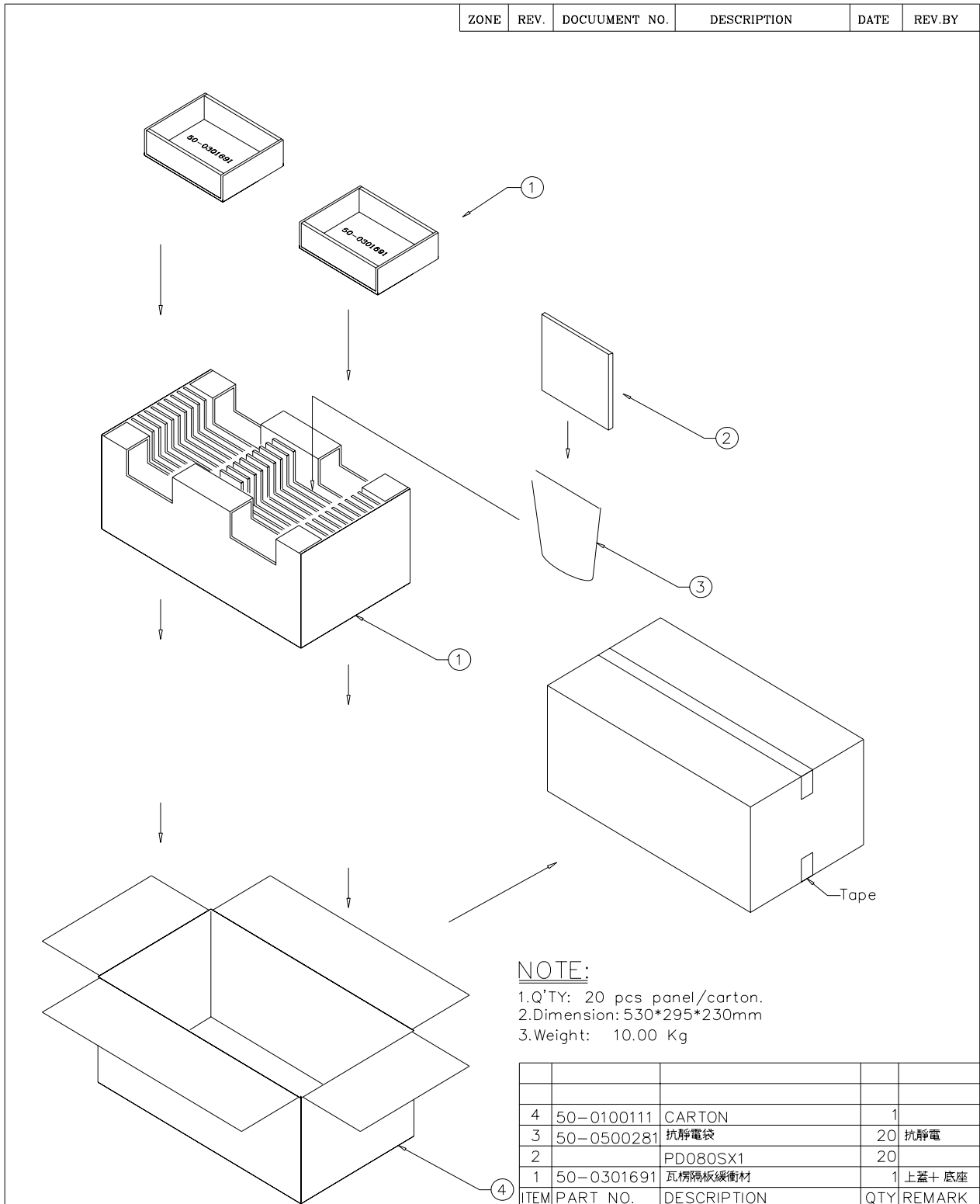
Ta: ambient temperature

Note: The protective film must be removed before temperature test

[Criteria]

In the standard conditions, there is not display function NG issue occurred. (Including: line defect ,no image). All the cosmetic specification is judged before the reliability stress.

16.Packing



| ITEM | PART NO. | DESCRIPTION | QTY | REMARK |
|------|------------|-------------|-----|--------|
| 4 | 50-0100111 | CARTON | 1 | |
| 3 | 50-0500281 | 抗靜電袋 | 20 | 抗靜電 |
| 2 | | PD080SX1 | 20 | |
| 1 | 50-0301691 | 瓦楞隔板緩衝材 | 1 | 上蓋+底座 |

| | | | | | | | |
|-----------|--------|-------------------|---------|--------|-----------|--|------------|
| MTL.SPEC. | | UNSPECIFIED TOL'S | | REMARK | | 元太科技工業股份有限公司 Prime View International Co., Ltd. | |
| | | ANGLE | | | | | |
| | | ROUGHNESS | | | | DWG.TITLE | |
| APPROVE | Franks | '06.12.12 | SCALE | UNIT | SHEET | PD080SX1 Packing Draw | |
| CHECK | Franks | '06.12.12 | | | 1 of 1 | | |
| DRAWN | Ethanc | '06.12.12 | MTL.NO. | | DWG FILE: | | REV. 01 |
| | | | | | | | A4 SIZE |

Revision History

| Rev. | Eng. | Issued Date | Revised Content |
|-------------|-------------|--------------------|------------------------|
| 0.1 | 黃秀晶 | Dec 08, 2006 | Preliminary |
| 1.0 | 黃秀晶 | Jan 12, 2006 | New |